

COMPAL CONFIDENTIAL

MODEL NAME : Bullseye TGL

PCB NO : DA6002EZ000

PCB 2X2 LA-K034P REV0 M/B 1 S

TGL-U+MEC1515  
(UMA)  
2021-03-08  
REV : 1.0 (A00)

TGL CPU QS

UC1  
SA0000DRS1L  
QS\_I3@  
S IC A31 FH8069004531502 QVBG B1 3G S

UC1  
SA0000DRR1L  
QS\_I5@  
S IC A31 FH8069004530601 QVBD B1 2.4G S

UC1  
SA0000DRG1L  
QS\_I7@  
S IC A31 FH8069004529905 QVBA B1 2.8G S

TGL CPU Base-U

UC1  
SA0000DXG0L  
PENTIUM@  
S IC A31 FH8069004531802 QVBK B1 2G S

UC1  
SA0000DXH0L  
CELERON@  
S IC A31 FH8069004531901 QVBS B1 1.8G S

TGL CPU R3

UC1  
SA0000DTV2L  
R3\_I3@  
S IC FH8069004531602 SRK08 B1 3G A31 !

UC1  
SA0000DTU2L  
R3\_I5@  
S IC FH8069004531301 SRK05 B1 2.4G A31 !

UC1  
SA0000DTT2L  
R3\_I7@  
S IC FH8069004530104 SRK02 B1 2.8G A31 !

DAZ part number  
DAZ2XB00101 - GCE  
DAZ2XB00102 - TRIPOD  
DAZ2XB00103 - HSB  
DAZ2XB00104 - TMT

@ : Un-pop Component  
UMA@ : not Support external Graphic card  
N3@/V3@ : Inspiron/Vostro  
MSFT@/NMSFT@ : MSFT SKU / Normal SKU  
G3@ : Support G3 sharing SPI topology  
CNV@ : Support CNVi function  
S5LID@/LID@ : Support S5 LID power up Function/Normal LID close  
ES\_I3@/ES\_I5A@/ES\_I5B@/QS\_I7@ : TGL-U QS Sample  
STG@ : C10\_gate control VCCSTG  
I2CTCH@/USBTCH@ : Touch Screen support I2C signal / USB signal  
BASE@/PREM@ : Pentium,Celeron/i3,i5,i7  
I2CPAD@/PS2PAD@ : EC use I2C touch PAD signal(or PS2)  
JP@/JUMP@/PJP@ : JUMP  
100@/1000@ : 10/100 LAN / Giga-LAN  
PRO@/ICPRO@ : only LCDVDD protection/Hinge up protection Support  
EMI@/ESD@/RF@ : EMI, ESD and RF Component  
@EMI@/@ESD@/@RF@ : EMI, ESD and RF Un-POP Component  
CMC@ : XDP Component  
CONN@ : Connector Component  
KBBL@ : KB Backlight  
TPM@/NTPM@ : HW TPM/SW TPM  
750\_CTPM@ : 750 and china TPM  
CTPM@/ST\_CTPM@ : China TPM/ST China TPM  
FFS@ : Free Fall Sensor  
TYPEC@/NTYPEC@ : Support TypeC/non-TypeC  
TYPEC@EMI@/TYPEC@ESD@ : EMI, ESD ,TypeC Component  
LBIST@/LBIST@RF@ : LBIST for LCD monitor  
TP@/CMC@TP@ : Test Point/XDP Test Point  
DISPCB@/UMAPCB@ : PCB MB

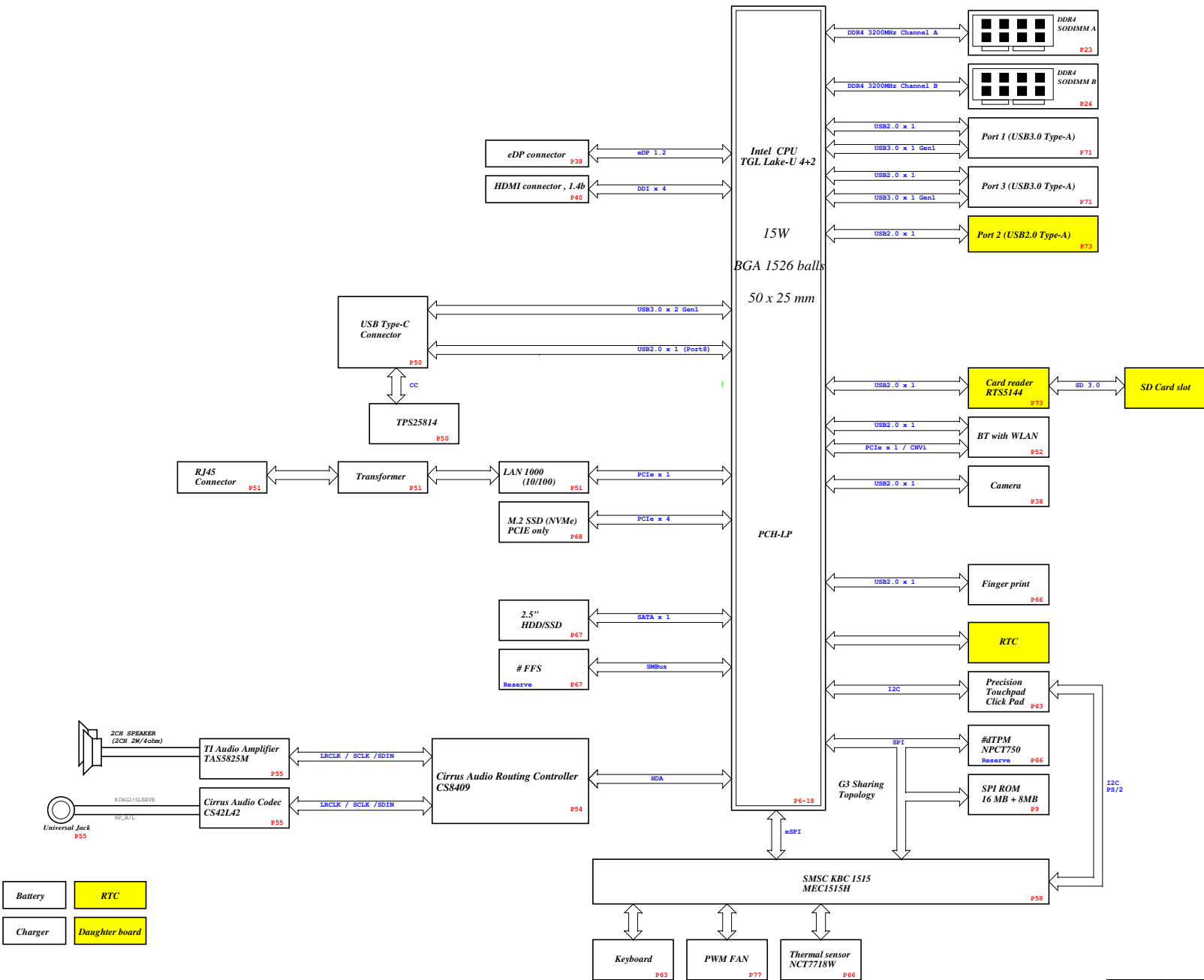
Layout Dell logo



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REV: X01  
PWB: 9HTP8

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Block Diagram



POWER STATES

Signal	SLP S3#	SLP S4#	SLP S5#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
State							
S0 (Full ON) / M0	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM) / M3	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M3	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M3	LOW	LOW	LOW	ON	OFF	OFF	OFF
G3	OFF	OFF	OFF	OFF	OFF	OFF	OFF
DS3	---	---	---	---	---	---	---

USB 2.0	DESTINATION
1	USB2.0 port1
2	USB2.0 Port2
3	USB2.0 port3, IO/B
4	Typec-C
5	Finger printer
6	CCD
7	Card reader , IO/B
8	Touch screen
9	Reserved
10	BT

Board ID & Model ID Table

Bullseye TGL			
	SKU	Model-ID (RE4 PD-100K)	Board-ID (RE2 PD-100K)
NBDR	UMA	RE3 PU-10K	RE1 PU-10K -EVT RE1 PU-17.8K -DVT1 RE1 PU-27.0K -Reserve RE1 PU-37.4K -DVT2 RE1 PU-49.9K -Reserve RE1 PU-64.9K -Pilot RE1 PU-82.5K -Reserve
	DSC - N175-G3	RE3 PU-17.8K	

Voltage Rails

Power Plane	Description	S0	S3	S4/S5	G3
+19V_ADPIIN	Adapter power supply	N/A	N/A	N/A	N/A
+17.4V_BATT++	Battery power supply	N/A	N/A	N/A	N/A
+19VB	AC or battery power rail for System	N/A	N/A	N/A	N/A
+RTC_SOC	RTC power	ON	ON	ON	ON
+3VALW_DSW	+3VALW power for PCH DSW rails	ON	ON	ON*	OFF
+5VALW	System +5V always on power rail	ON	ON	ON*	OFF
+3VALW	System +3V always on power rail	ON	ON	ON*	OFF
+1.8V_PRIM	System +1.8V always on power rail	ON	ON	ON*	OFF
+1.0V_PRIM	System +1.0V always on power rail	ON	ON	ON*	OFF
+1.2V_DDR	DDR4 +1.2V power rail	ON	ON	OFF	OFF
+2.5V_MEM	DDR4 +2.5V power rail	ON	ON	OFF	OFF
+0.6V_DDR_VTT	DDR +0.6VS power rail for DDR terminator	ON	OFF	OFF	OFF
+VCCIN_AUX	CPU and PCH merged auxiliary power rail	ON	ON	ON	OFF
+VCCST	+1.05 VCCST power rail	ON	ON	ON	OFF
+VCCSTG	+1.05 VCCSTG power rail	ON	OFF	OFF	OFF
VCCPLL	+1.05 VCCPLL power rail	ON	ON	ON	OFF
+VCC_IN	Core voltage for CPU	ON	OFF	OFF	OFF
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON	OFF
+3VALW_DSW	+19VB to DSW power rail for suspend power	ON	ON	ON	OFF
+3VALW_PCH	+3VALW power for PCH suspend rails	ON	ON	ON*	OFF
+5VS	System +5VS power rail	ON	OFF	OFF	OFF
+3VS	System +3VS power rail	ON	OFF	OFF	OFF
+1.35V_MEM GFX	+1.35V power rail for GPU	ON	OFF	OFF	OFF
+3VGS	+3V power rail for GPU	ON	OFF	OFF	OFF
+1.8VGS	+1.8V power rail for GPU	ON	OFF	OFF	OFF
+0.95VSDGPU	+0.95V power rail for GPU	ON	OFF	OFF	OFF

Note : ON\* means that this power plane is ON only with AC power available, otherwise it is OFF

RE: ICL N3V3 MLK High Power Consumption on VCCIN\_AUX Under S3/S5

Wu, Eddie <eddie.wu@intel.com>

寄件日期: 2019/5/6 (星期四) 下午 09:41

收件人: Chen, Deval (TFB); Chen, Johany (TFB); Hong, Henry (TFB); Chang, Iay Si; Lau, Joe (TFB); Lai, Carol (TFB); Krazy, Lu@del.com

副本: Chen, AlexCL (TFB); Chang, Gary; Hase, Jimmy

Hi David,  
VCCIN\_AUX only down to 0V while SLP\_S0# is asserted.  
On S3 mode, it only can down to 1.1V. Thanks.

Best Regards,  
Eddie Wu +886-2-66221110

10.12.4 Power States

Table 207. System with M3 State Supported

Rails	SKUs	S0/M0 3	C102	S0ix/M-off*	S3/M3	S3/M-off	S4 and S5/M3	S4 and S5/M-off	Deep S4/S5	G3+
VCCRTC	All	ON	ON	ON	ON	ON	ON	ON	ON	ON
VCCDSW_WP3	All	ON	ON	ON	ON	ON	ON	ON	ON	No Power
VBATA (VDC)	All	ON	ON	ON	ON	ON	ON	ON	ON	No Power
V5.0A	All	ON	ON	ON	ON	ON	ON	ON	OFF	No Power
VCCPRIM_WP3	All	ON	ON	ON	ON	ON	ON	ON	OFF	No Power
VCCPRIM_1P8	All	ON	ON	ON	ON	ON	ON	ON	OFF	No Power
VCC_VNNEXT_1 P05	All	ON	ON	ON	ON	ON	ON	ON	OFF	No Power
VCC_V1P0SEXT_1P05	All	ON	ON	ON	ON	ON	ON	ON	OFF	No Power
V3.3M <sup>5</sup>	All	ON	ON	OFF	ON <sup>10</sup>	OFF	ON <sup>10</sup>	OFF	OFF	No Power
V1.8M <sup>5</sup>	All	ON	ON	OFF	ON <sup>10</sup>	OFF	ON <sup>10</sup>	OFF	OFF	No Power
VDDQ	All	ON	ON	ON	ON	ON	OFF	OFF	OFF	No Power
V2.5U (VPP)	All	ON	ON	ON	ON	ON	OFF	OFF	OFF	No Power
VCCST	All	ON	ON	ON	ON <sup>13</sup>	ON <sup>13</sup>	OFF <sup>6</sup>	OFF <sup>6</sup>	OFF	No Power
VCCSTG	All	ON	OFF <sup>2</sup>	OFF	OFF	OFF	OFF	OFF	OFF	No Power
V3.3S	All	ON	ON	ON	OFF	OFF	OFF	OFF	OFF	No Power
VCCIN	All	ON	ON	ON <sup>11</sup>	OFF	OFF	OFF	OFF	OFF	No Power
VCCIN_AUX	All	ON	ON	ON <sup>11</sup>	OFF <sup>14</sup>	OFF <sup>14</sup>	OFF <sup>14</sup>	OFF <sup>14</sup>	OFF	No Power

Note : VCCIN\_AUX only down to 0V while SLP\_S0# is asserted. On S3 mode, it only can down to 1.1V.

USB3.0	PCIE	SATA	DESTINATION
USB3.0-1	PCIE-1		USB3.0 (MB)(Type-A)
USB3.0-2	PCIE-2		USB3.0 (MB)(Type-A)
USB3.0-3	PCIE-3		USB3.0 (Type-C)
USB3.0-4	PCIE-4		USB3.0 (Type-C)
	PCIE-5		PCIE SSD
	PCIE-6		PCIE SSD
	PCIE-7		PCIE SSD
	PCIE-8		PCIE SSD
	PCIE-9		LOM
	PCIE-10		WLAN
	PCIE-11	SATA-0	SATA HDD
	PCIE-12	SATA-1	NC
	PCIE4 - 0		NC
	PCIE4 - 1		NC
	PCIE4 - 2		NC
	PCIE4 - 3		NC

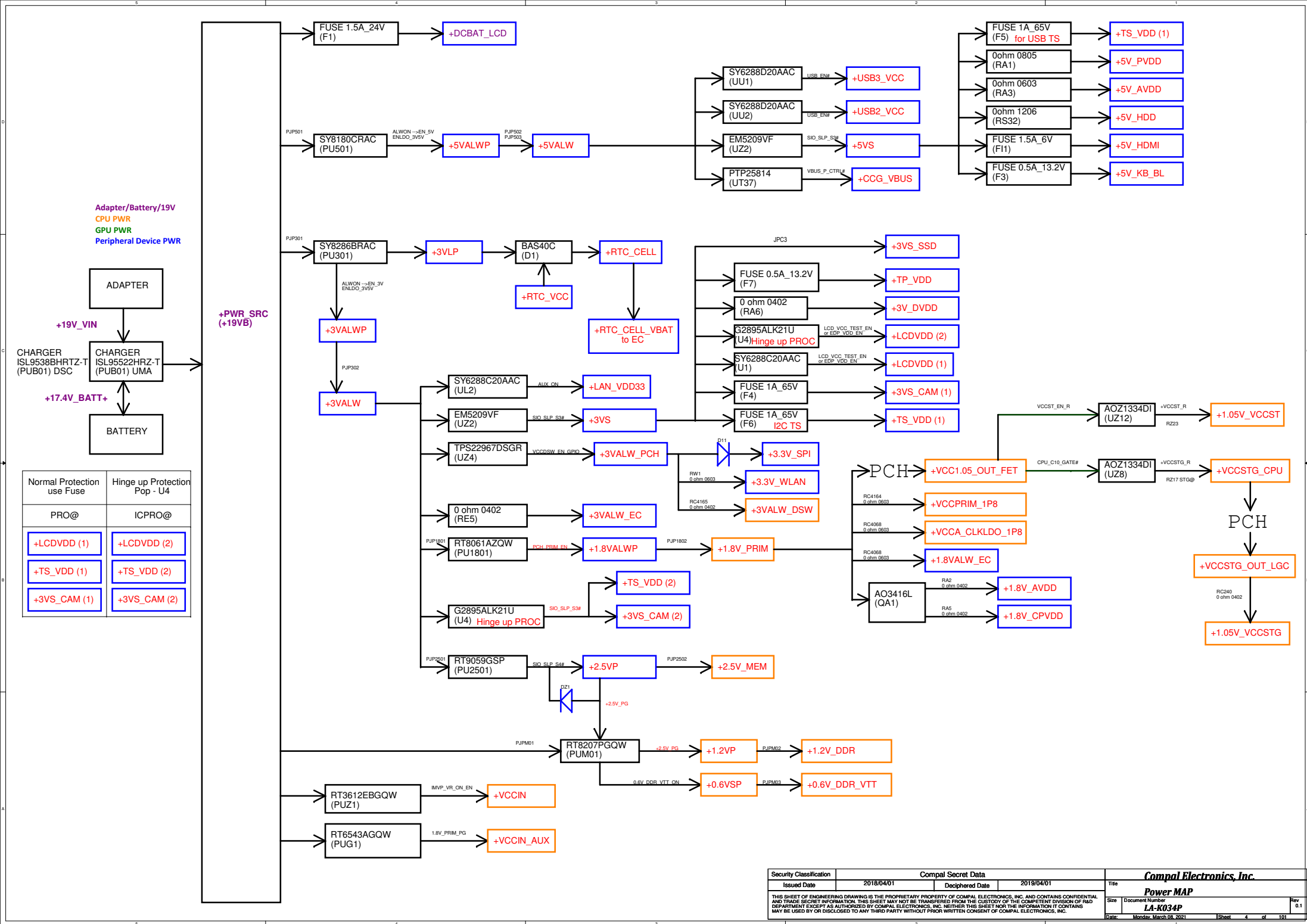
Figure 77. High Speed I/O (HSIO) Lane Multiplexing in PCH-LP (UP3)

Flex HSIO Lane	0	1	2	3	4	5	6	7	8	9	10	11
HSIO Type and Lane	USB 3.2 Gen 1x1/2x1 #1	USB 3.2 Gen 1x1/2x1 #2	USB 3.2 Gen 1x1/2x1 #3	USB 3.2 Gen 1x1/2x1 #4	PCIE* #5	PCIE* #6	PCIE* #7	PCIE* #8	PCIE* #9	PCIE* #10	PCIE* #11	PCIE* #12

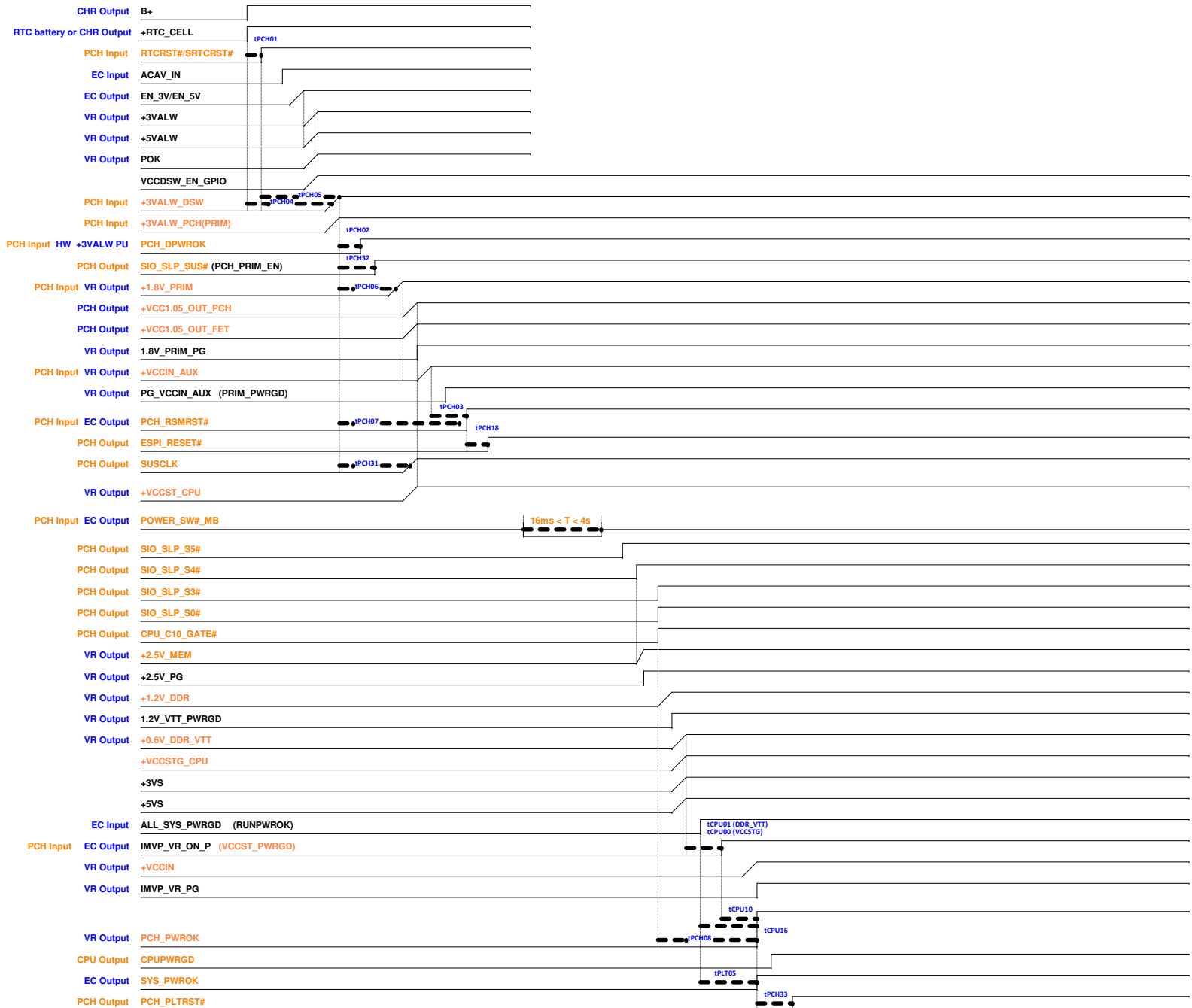
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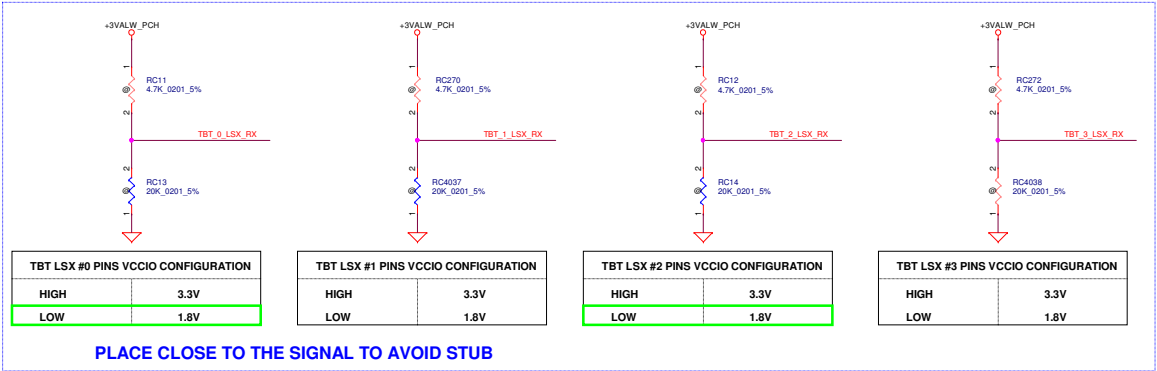
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Power Up Sequence  
G3 to S0

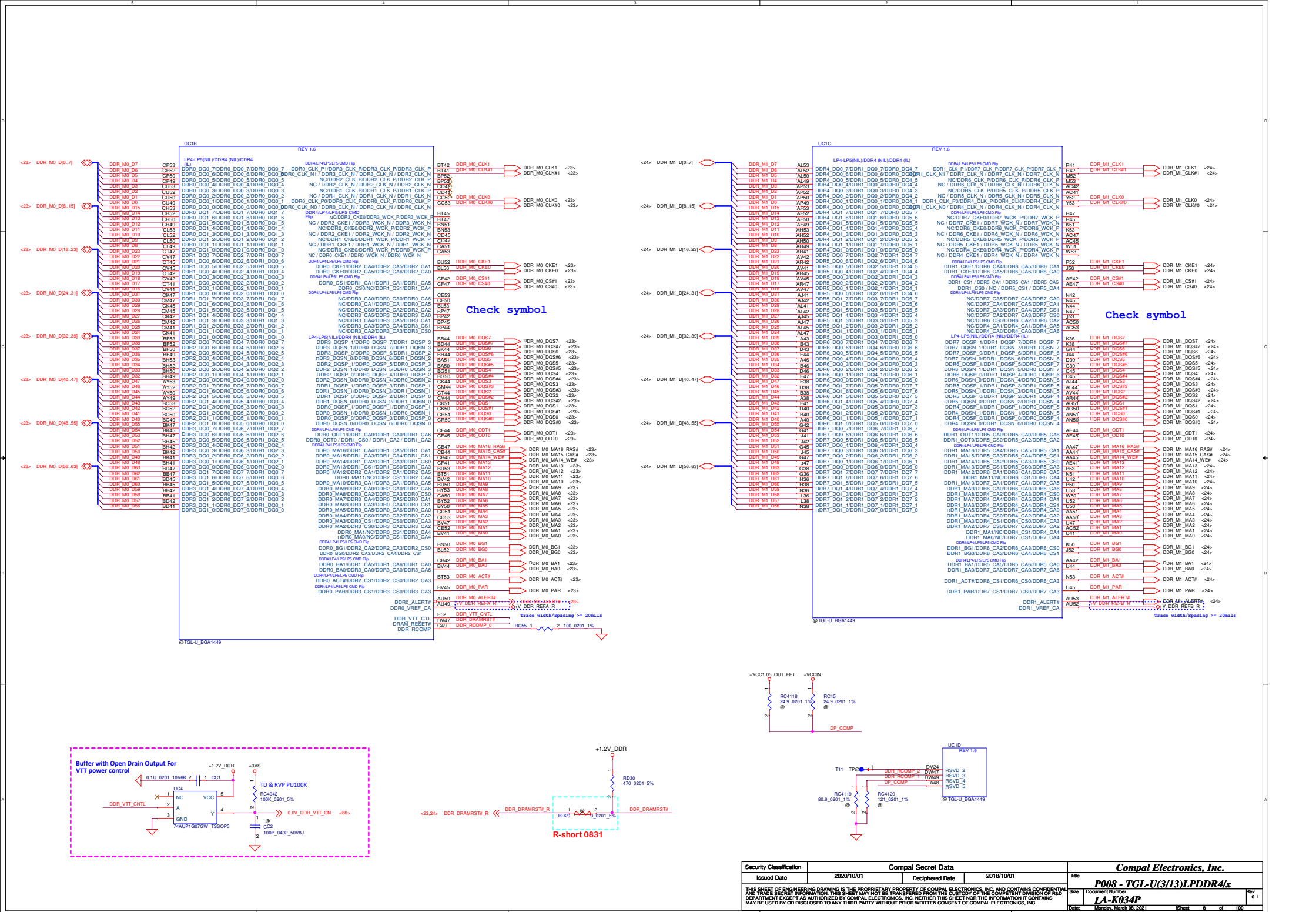




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## TOP SWAP OVERRIDE

GPP\_B14 / SPKR (Internal 20 K Pull Down)

0 = Disable "Top Swap" mode. (Default)

1 = Enable "Top Swap" mode.

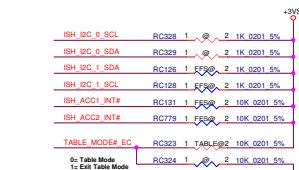
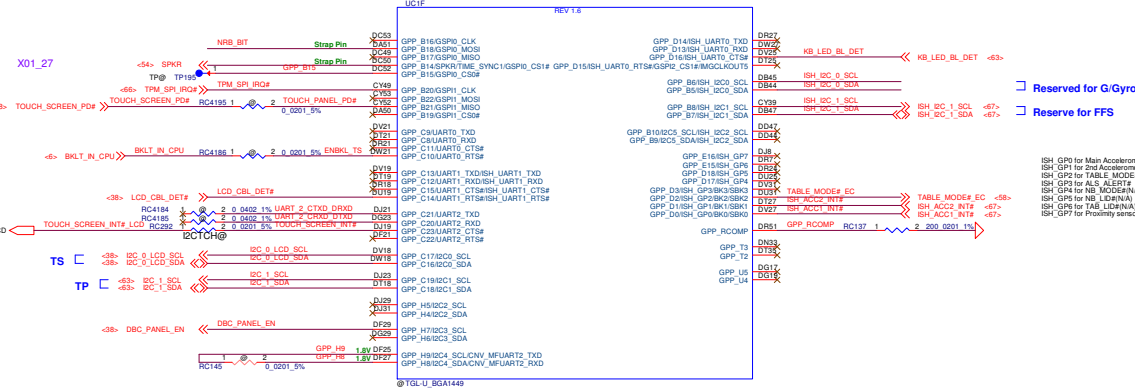


## NO REBOOT

GPP\_B18/GSP10\_MOS (Internal 20 K Pull Down)

0 = REBOOT ENABLED

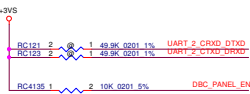
1 = NO REBOOT (This function is useful when running ITP/XDP).



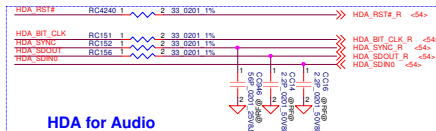
Reserved for Gi/Gyo  
Reserve for FFS

ISH\_GPP for Main Accelerometer (KB Board)INT#  
ISH\_GPP for 2nd Accelerometer (Camera Board)INT#  
ISH\_GPP for TABLE\_MODE#  
ISH\_GPP for ALS\_ALERT#  
ISH\_GPP for NB\_MODERNA(A)  
ISH\_GPP for TAB\_LIDAR(A)  
ISH\_GPP for TAB\_LIDAR(B)  
ISH\_GPP for Proximity sensor(Camera)INT#

Place near JWLAN1



## HDA for Audio

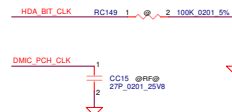
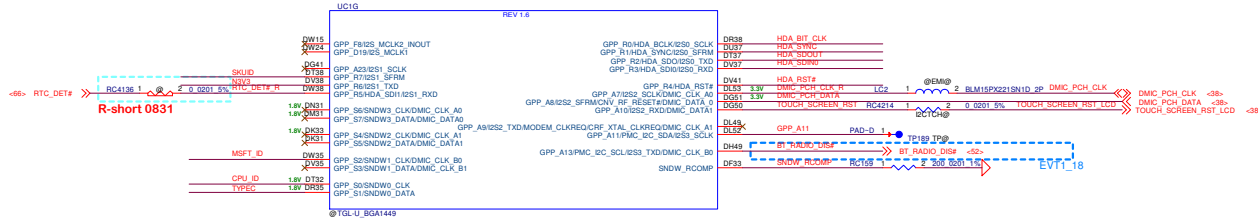


## FLASH DESCRIPTOR SECURITY OVERRIDE

GPP\_R2/HDA\_SDO (Internal 20 K Pull Down)

0 = ENABLE (DEFAULT)

1 = DISABLE (ME can update)



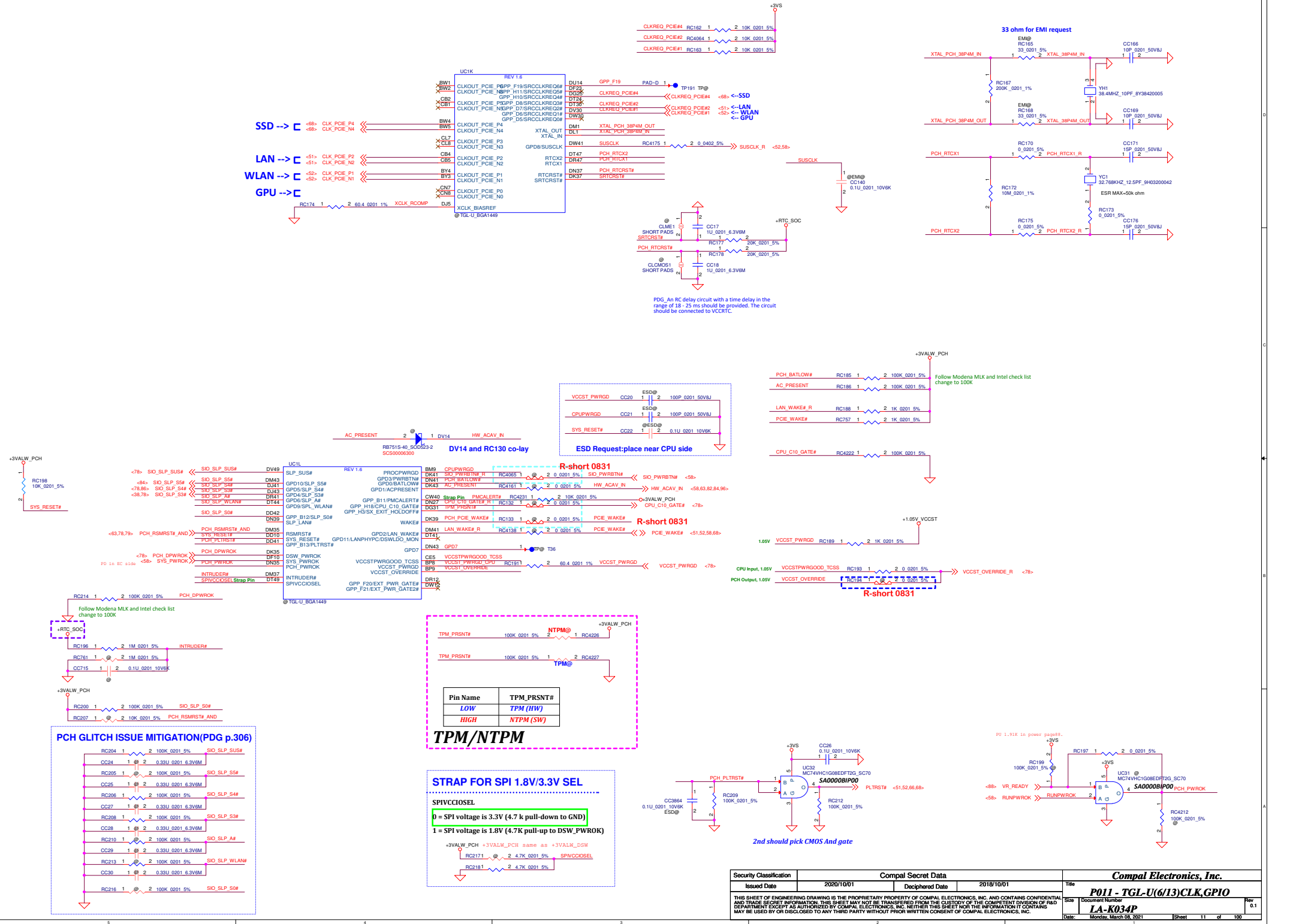
Pin Name	MSFT_ID
LOW	Realtek
HIGH	Cirrus

Pin Name	Net name : N3V3
2nd source	Audio control change to MSFT control (Default)
main source	Audio control change to MSFT control

SKUID	UMA@	LOW
	DIS@	DSC

Pin Name	CPU_ID	TYPEC
LOW	Base-U	Non-TYPEC
HIGH	Premium-U	TYPEC

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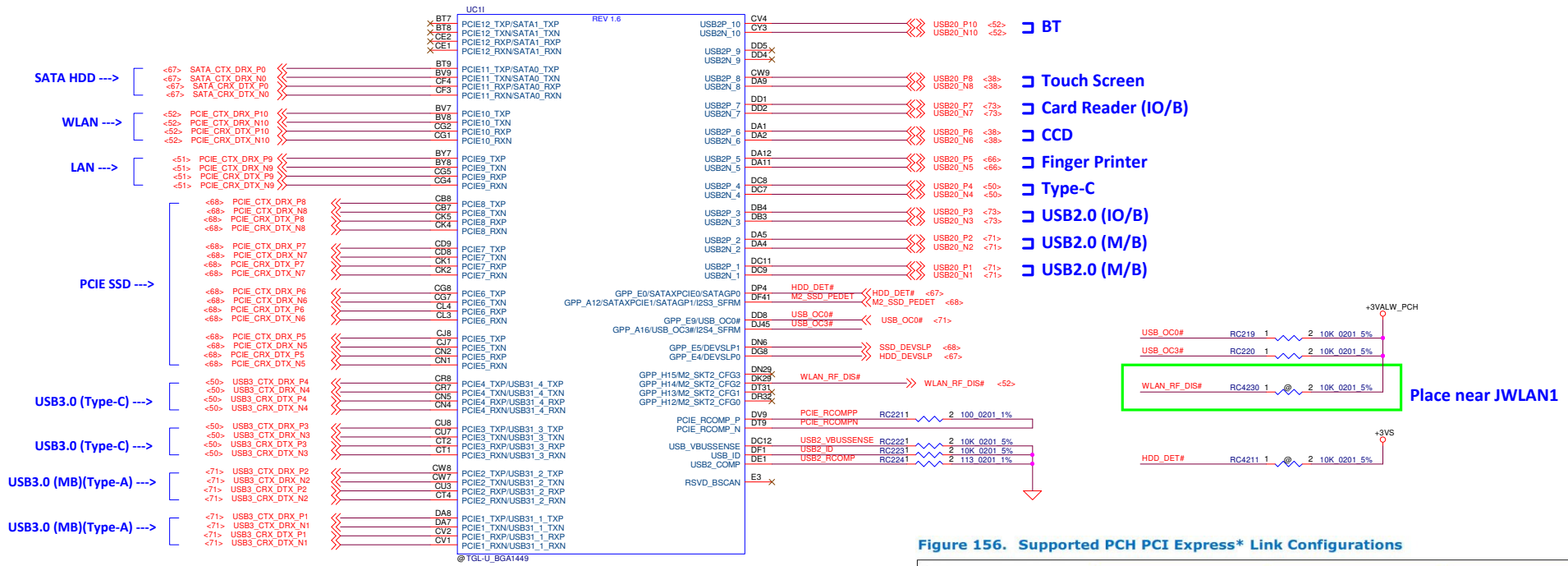
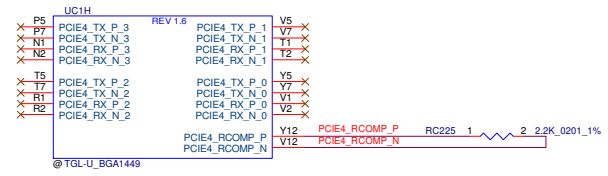
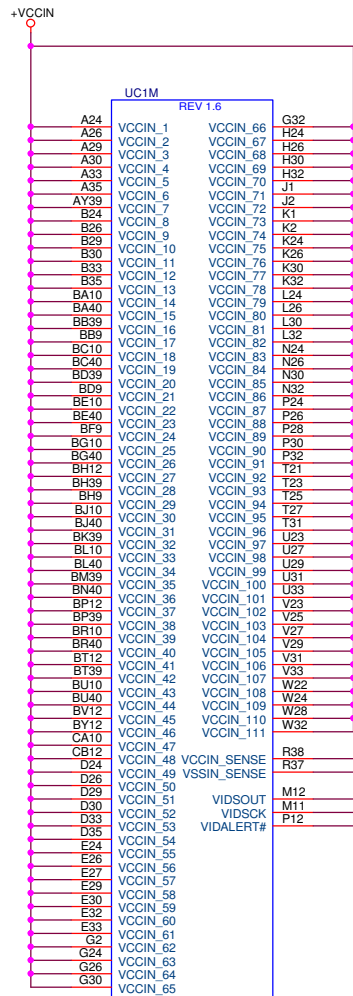


Figure 156. Supported PCH PCI Express\* Link Configurations

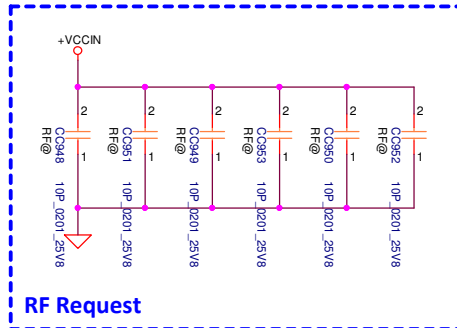
PCH-LP		PCIe* Controller #1				PCIe* Controller #2				PCIe* Controller #3					
Flex I/O Lanes		0	1	2	3	4	5	6	7	8	9	10	11		
PCIe* Lanes		1	2	3	4	5	6	7	8	9	10	11	12		
Link Lanes	1x4	0	1	2	3	0	1	2	3	0	1	2	3		
	1x4 LR	3	2	1	0	3	2	1	0	3	2	1	0		
	2x2	0	1	0	1	0	1	0	1	0	1	0	1		
	1x2+2x1	0	1	0	0	0	1	0	0	0	1	0	0		
	2x1+1x2	0	0	1	0	0	0	1	0	0	0	1	0		
	4x1	0	0	0	0	0	0	0	0	0	0	0	0		
Base-U	1x4					RP5				RP9					
	1x4 LR					RP5				RP9					
	2x2					RP5		RP7		RP9		RP11			
	1x2+2x1					RP5		RP7	RP8	RP9		RP11	RP12		
	2x1+1x2					RP8	RP7	RP5		RP12	RP11	RP9			
	4x1					RP5	RP6	RP7	RP8	RP9	RP10	RP11	RP12		
Premium-U	1x4	RP1				RP5				RP9					
	1x4 LR	RP1				RP5				RP9					
	2x2	RP1		RP3		RP5		RP7		RP9		RP11			
	1x2+2x1	RP1		RP3	RP4	RP5		RP7	RP8	RP9		RP11	RP12		
	2x1+1x2	RP4	RP3	RP1		RP8	RP7	RP5		RP12	RP11	RP9			
	4x1	RP1	RP2	RP3	RP4	RP5	RP6	RP7	RP8	RP9	RP10	RP11	RP12		
Premium-Y	1x4	RP1								RP9					
	1x4 LR	RP1								RP9					
	2x2	RP1		RP3						RP7		RP9		RP11	
	1x2+2x1	RP1		RP3	RP4					RP7	RP8	RP9		RP11	RP12
	2x1+1x2	RP4	RP3	RP1								RP12	RP11	RP9	
	4x1	RP1	RP2	RP3	RP4					RP7	RP8	RP9	RP10	RP11	RP12







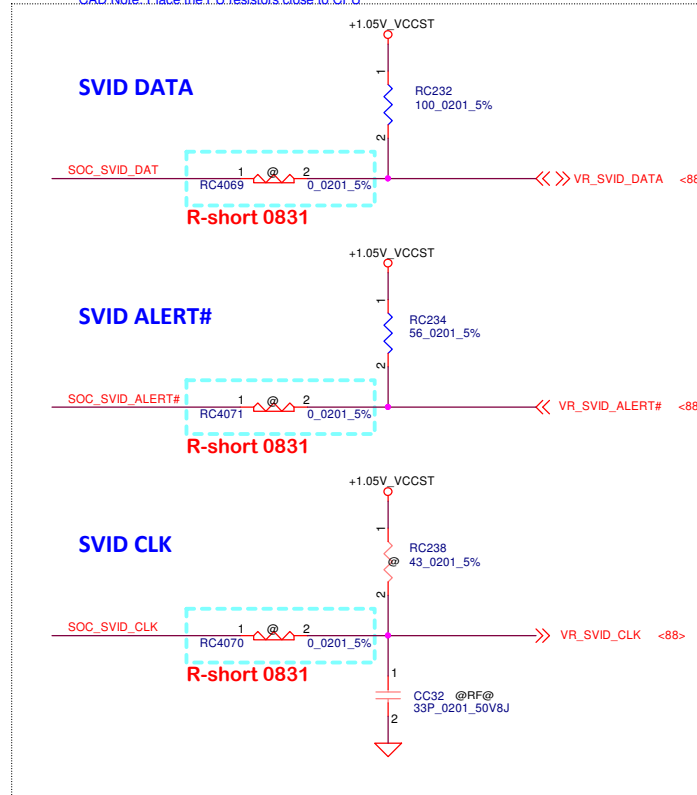
@TGL-U\_BGA1449



Trace Length Match<25 mils  
Must be routed as differential pair to VR

VCC\_SENSE\_VCCIN <88>  
VSS\_SENSE\_VCCIN <88>

- 1.The total Length of Data and Clock (from CPU to each VR) must be equal (±0.1 inch).
  - 2.Route the Alert signal between the Clock and the Data signals.
- CAD Note: Place the PU resistors close to CPU.

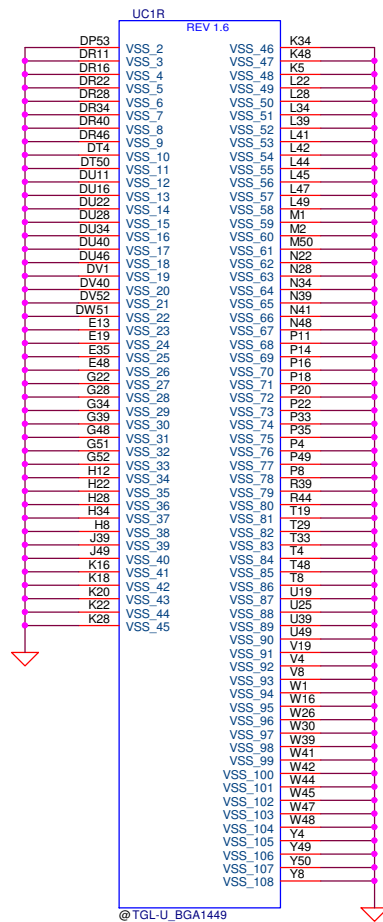
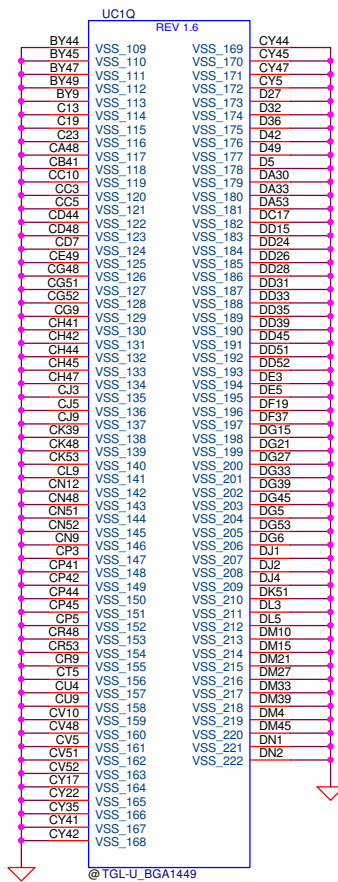
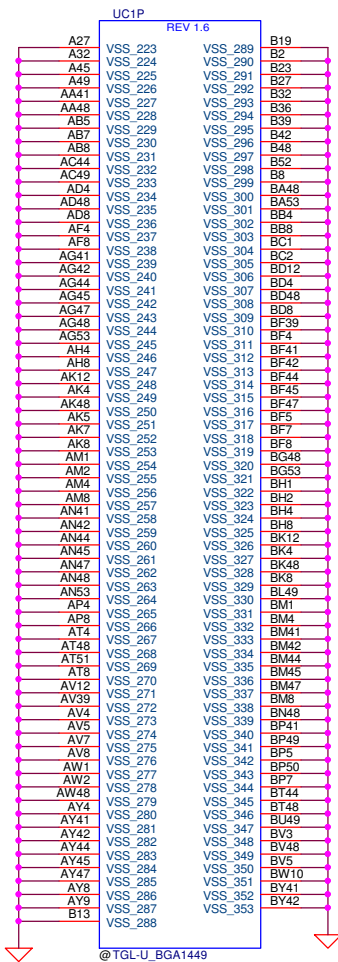


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				LA-K034P	



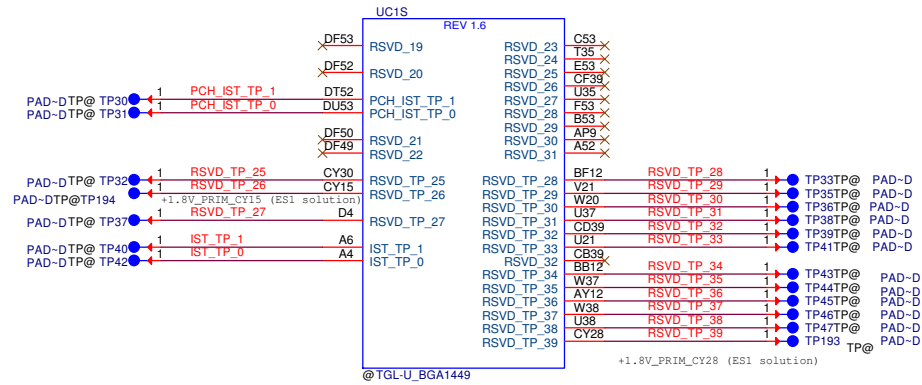






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								Size	Document Number	Rev
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ES1 Workaround Circuit  
Intel Document Number: 614056



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					LA-K034P	0.1
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Main Function:

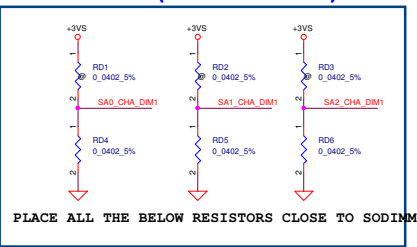
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# CHANNEL-M0

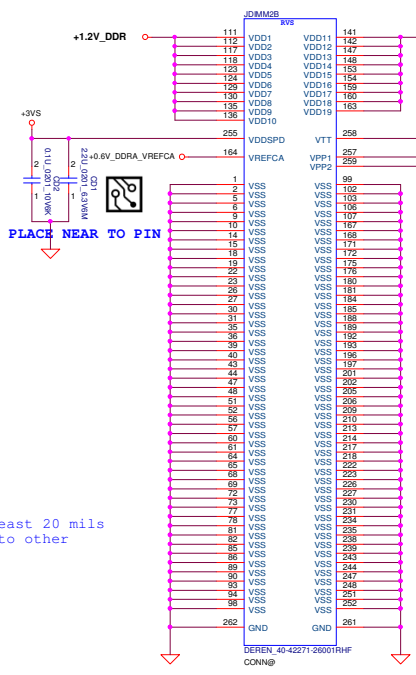
BOT: DIMM1 (JDIMM2 CONN) Non-ECC DIMM



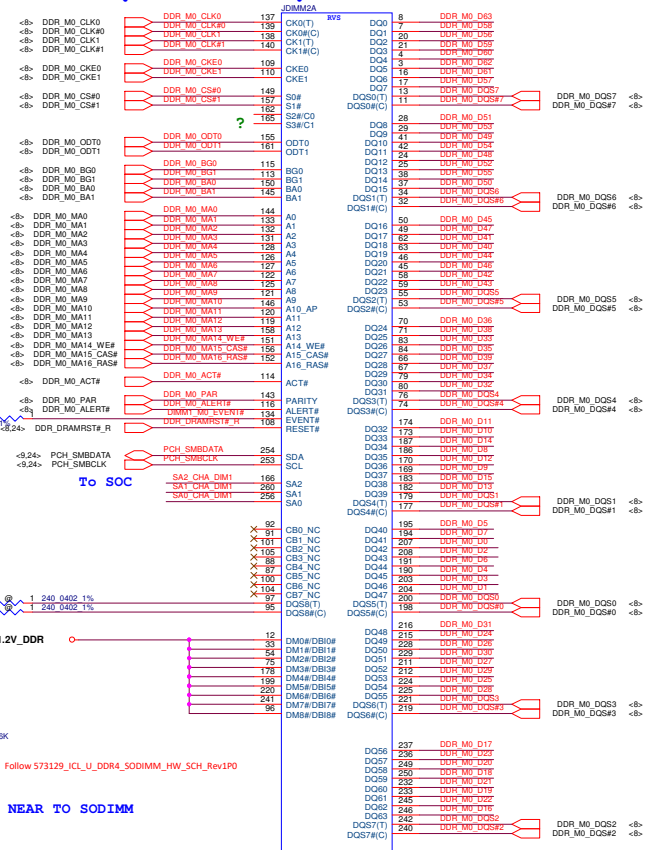
SPD ADDRESS FOR CHANNEL A :

SA0 = 0; SA1 = 0; SA2 = 0.

## Non-Interleaved Memory

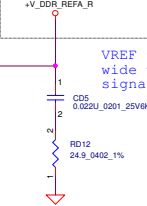


## REVERSE TYPE (5.2 mm)



### DIMM Side

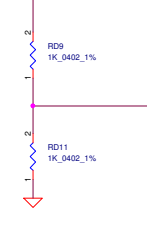
+0.6V\_DDR\_A\_VREFCA



VREF traces should be at least 20 mils wide with 20 mils spacing to other signals

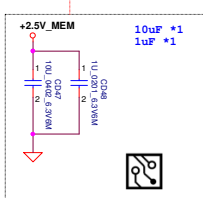


+1.2V\_DDR

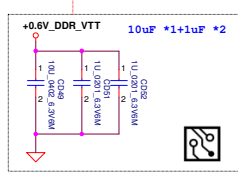


### Decoupling Cap\_Channel A

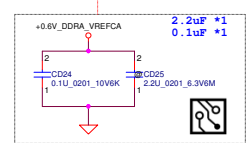
Layout Note: Place near JDIMM2. 257, 259



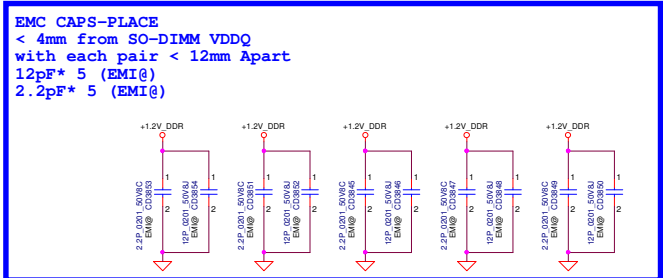
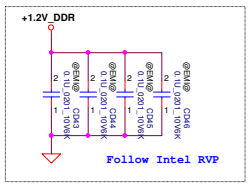
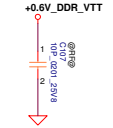
Layout Note: Place near JDIMM2. 258



Layout Note: PLACE THE CAP near JDIMM2. 164



C107 place near JDIMM2



Part Number:SP07001JH00  
Part Value:S SOCKET LOTES ADDR0208-P001A 260P DDR4

POP  
EMI@  
UNPOP  
@EMI@ESD@RF@CONN@



Main Function:

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Main Func = GPU

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Issued Date	2018/08/31	Deciphered Date	2019/08/06	Title	NV(1/5)-PCIE
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Main Func = GPU

Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2018/08/31	Deciphered Date	2019/08/06	Title	NV(2/5)-IFP ABCDEF DAC XTAL	
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Main Func = GPU

Security Classification	Compal Secret Data			Compal Electronics, Inc.	
Issued Date	2018/08/31	Deciphered Date	2019/08/06	Title	NV(3/5)-POWER
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Main Func = GPU



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Main Func = GPU

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Issued Date	2018/08/31	Deciphered Date	2019/08/06	Title	NV(S/S)-MEMORY FBA
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Main Func = VRAM

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				LA-K034P			0.1
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Main Func = VRAM

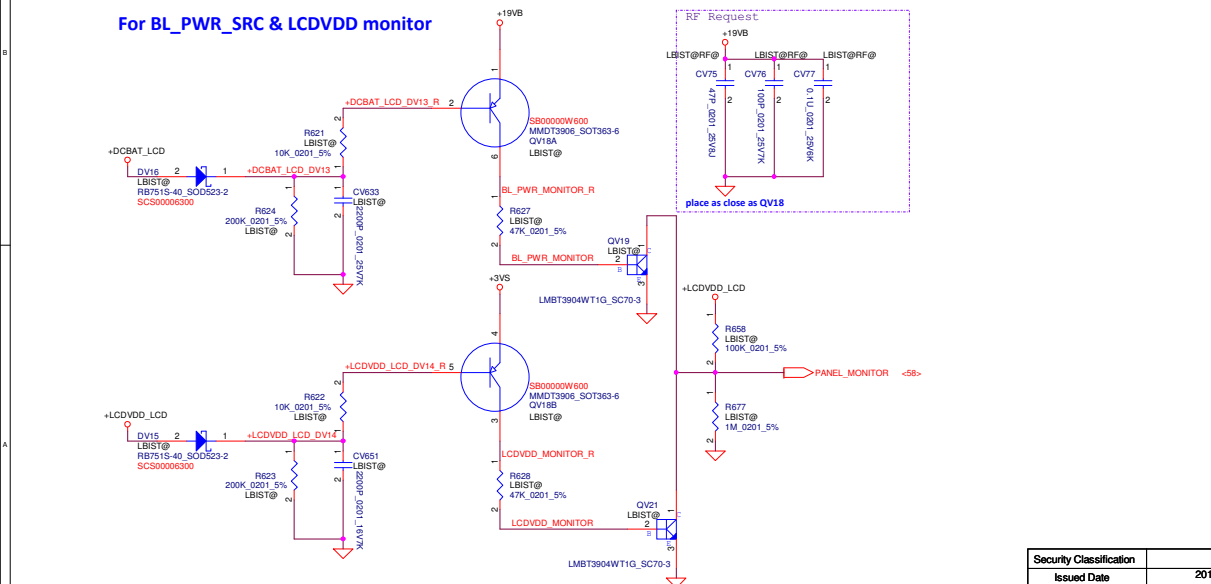
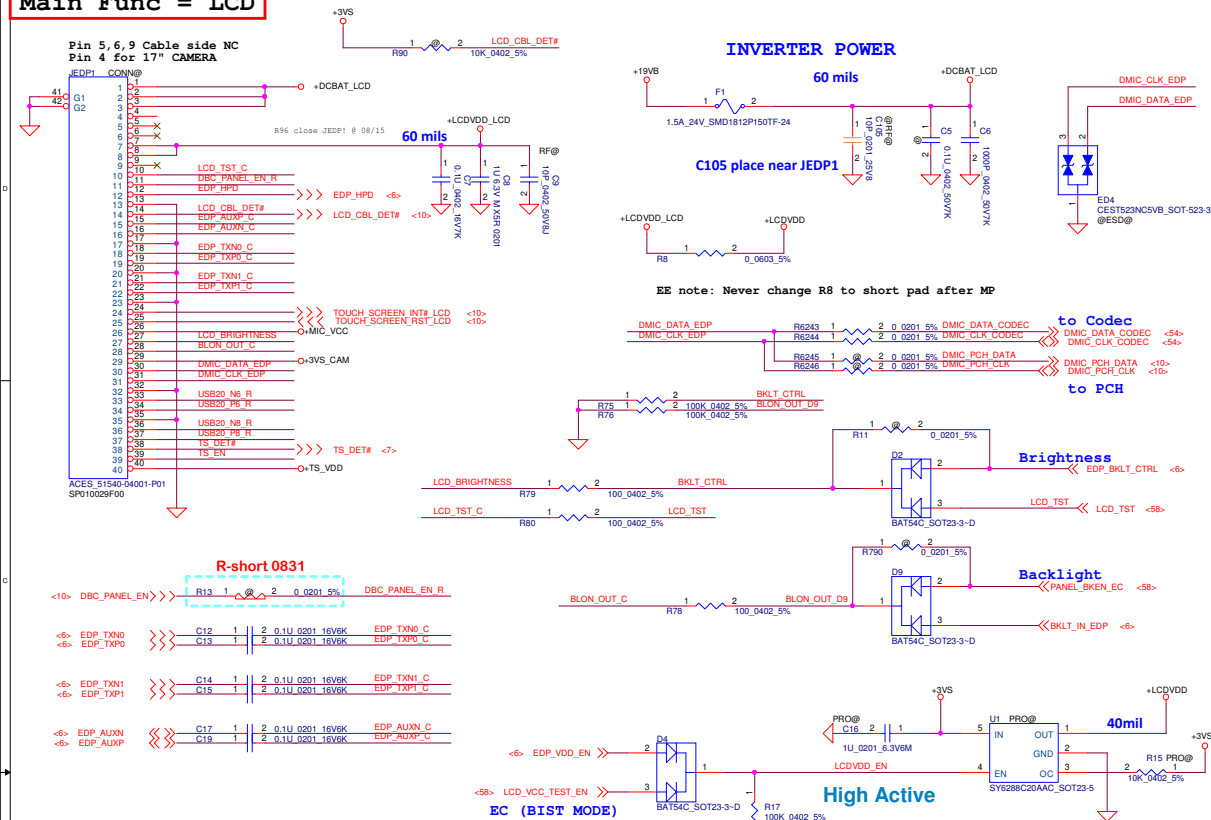
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2018/08/31	Deciphered Date	2019/08/06	Title	N17S_GDDR5_B	
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Main Func = GPU DC

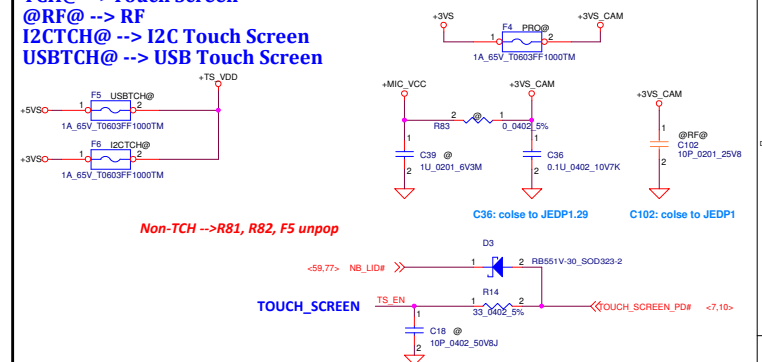
Security Classification	Compal Secret Data			Title	
Issued Date	2018/08/31	Deciphered Date	2019/08/06	DGPU DC/DC Interface	
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				LA-K034P	0.1
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# Main Func = LCD

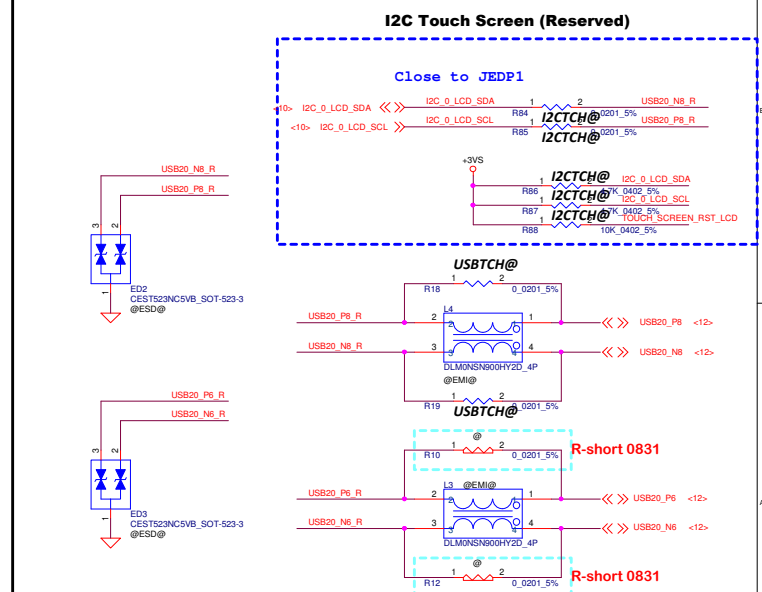
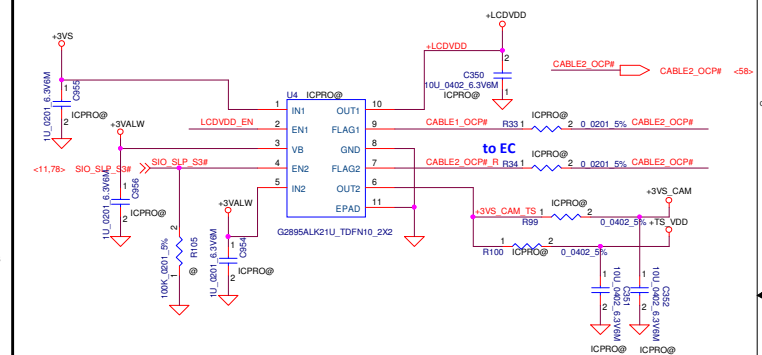


# Main Func = CAM&MIC, TS

TCH@ --> Touch Screen  
 @RF@ --> RF  
 I2CTCH@ --> I2C Touch Screen  
 USBTCH@ --> USB Touch Screen



# Main Func = Hinge up protection



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Main Func =

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				Sheet	46 of 101
				Rev	0.1

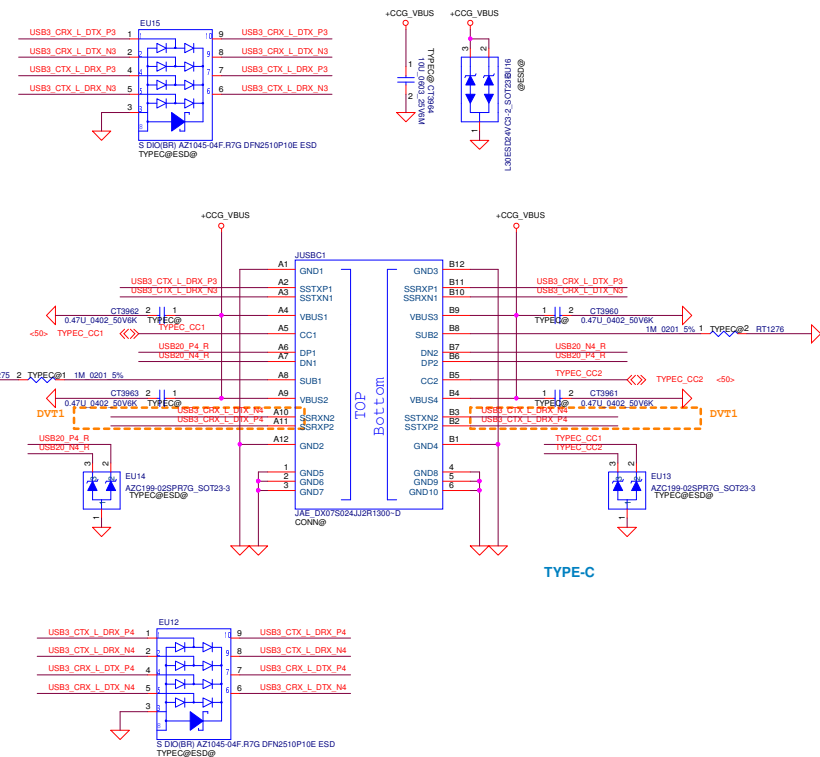
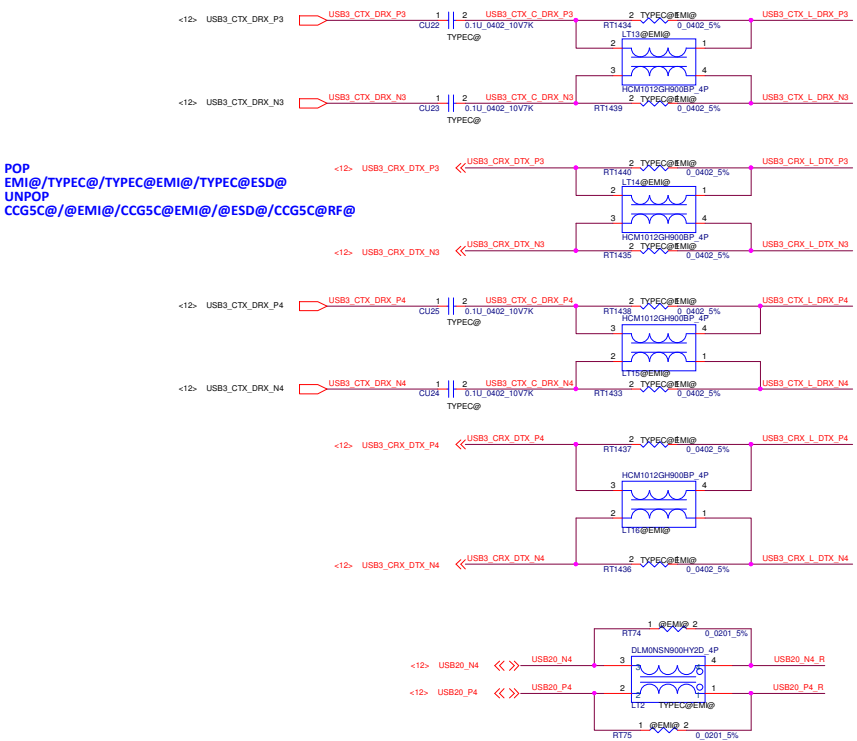
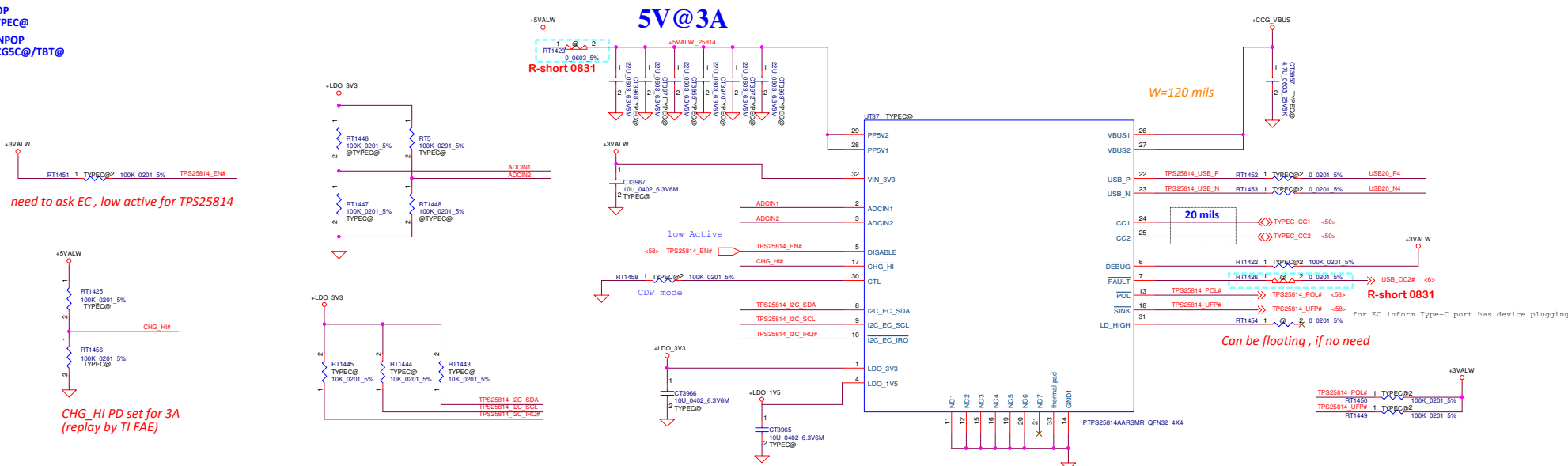
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Reserve



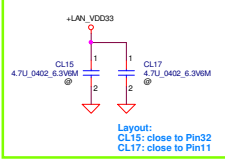
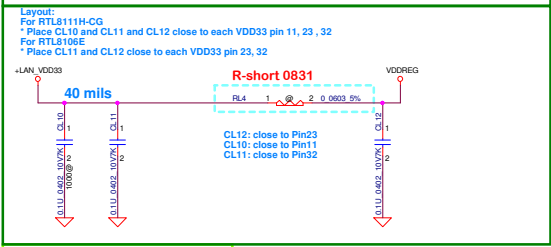
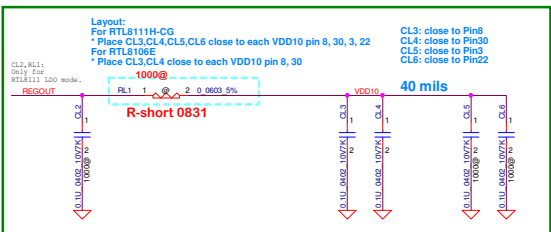
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				Rev	0.1

POP  
TYPEC@  
UNPOP  
CCG5C@/TBT@

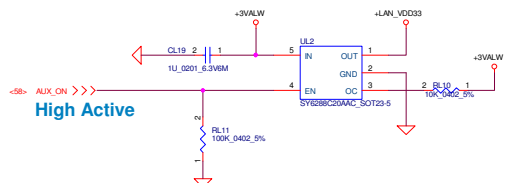
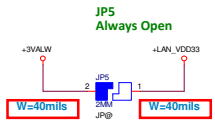


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Main Func = LAN

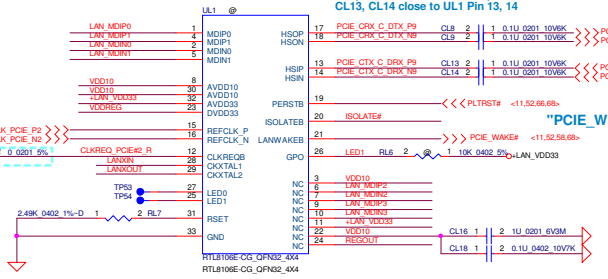
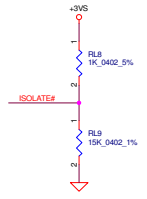
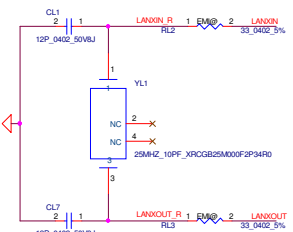
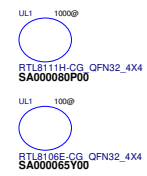


+LAN\_VDD33 Rising time (10%~90%) need >0.5mS and <100mS.



LAN CHIP 10/100/1000

RTL8111H-CG	RTL8106E-CG
SA000080P00	SA000065Y00
LDO mode	LDO mode
10/100/1000M	10/100M

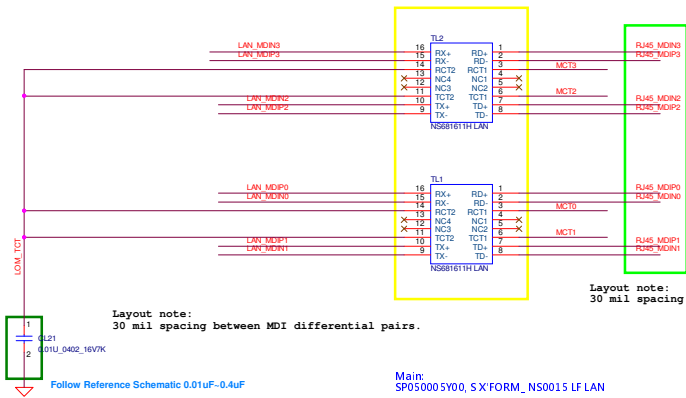


CL8, CL9 close to UL1 Pin 17, 18  
CL13, CL14 close to UL1 Pin 13, 14

"PCIE\_WAKE#" PU 1k on CPU side

Main Func = LAN LAN Transformer 10/100M x2

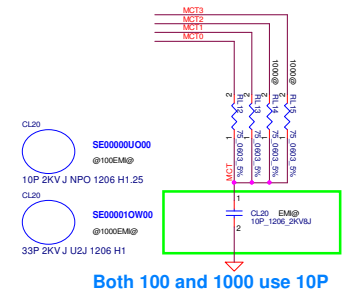
TL1 TOP, TL2 BOT



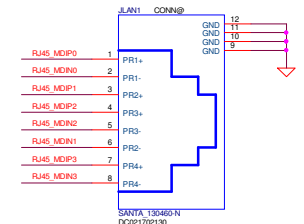
Layout note:  
30 mil spacing between MDI differential pairs.

Layout note:  
30 mil spacing between MDI differential pairs.

Main:  
SP050005Y00, S'X'FORM, NS0015 LF LAN



Both 100 and 1000 use 10P



	1.0V Source	RL1	CL2	CL5	CL6	CL10	CL12
RTL8111H-CG RTL8111G-CGT (71.08111.U03)	LDO	O	O	O	O	O	X
RTL8106E-CG (071.08106.0003)	LDO	X	X	X	X	X	O

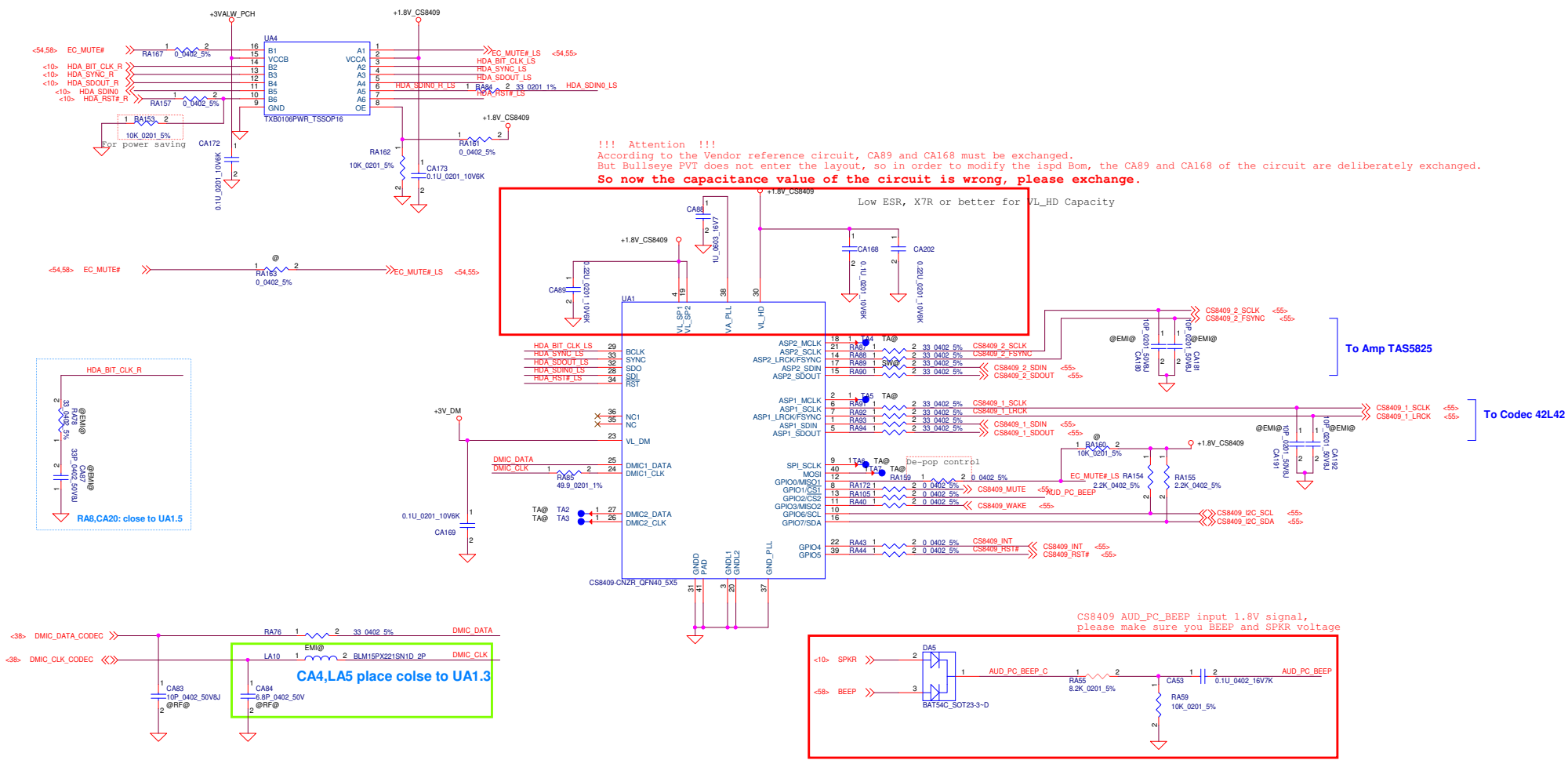




# Reserve

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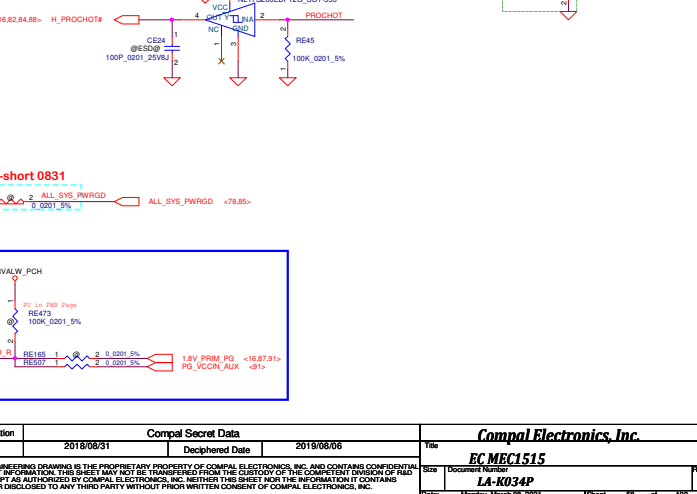
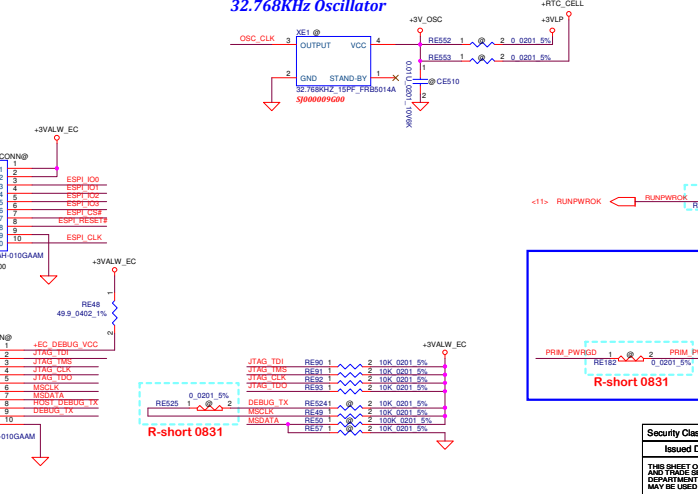
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Issued Date		Deciphered Date		Title			
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				Date		Date	
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PIN No	Strap Name	Strap define and value	I/O Power rail
GPI017	JTAG_STRAP	1=Use the JAG TAP Controller for Boundary Scan 0=The JTAG TAP Controller is used for debug (normal operation)	VT1R1
GPI014	VTREF_STRAP	Voltage Level strap is used to determine if the Shared Flash Interface must be configured for 3.3V or 1.8V operation 1= 3.3V Operation 0= 1.8V Operation	VT1R1
GPI0045	CR_STRAP	Crisis Recovery Strap 1=Normal Boot Source 0=Use the Private SPI pins to boot from Crisis Recovery flash over Keyscan connector Note: This pin requires an external pull-up for normal operation	VT1R1
GPI0207	CMP_STRAP	CMP_STRAP is the Comparator 0 Strap pin. This strap must be enabled in EFUSE (=Hardware Default) (GPIO input) 1=Comparator 0 Enabled 0=Comparator 0 Disabled	VT1R1
GPI0055/SHD_CS	BSS_STRAP_0W	Boot Source Select Strap 1=Use the Shared SPI pins for Boot 0=Use the eSPI Flash Channel for Boot	VT2R2
GPI0225/SHD_I2C0	PWNGRD_STRAP	Primary Power rails Good 1 = Primary power rails are good 0 = Primary power rails not stable	VT2R2





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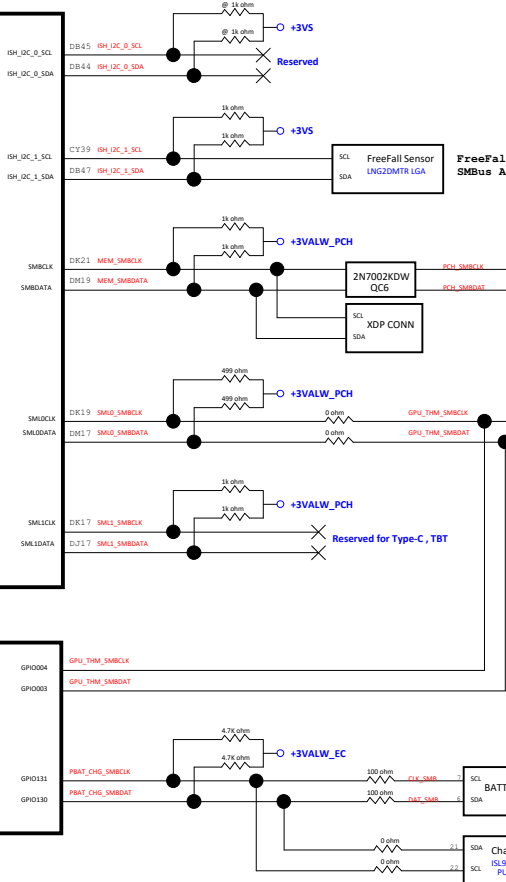


4.1 General Specifications			
This contents provide general characteristics for the model of PM2002.			
General Specifications	Item	Specs	Notes
	System	Self-Configuration type	
	Multi-Track Points	10 points	
	Active track area	Same as 1000 series	
	Type	Advanced Self-Track Switch	
	Storage Chamber (Depth)	4.5mm (2) x 3.5mm (2)	
	Power	MT 4710	Monitor
	Input-IC Information	Formulated see <a href="#">IC-100</a>	(N/A)
	PC	MT10	
	IC	MT10	
Number of Storage Chamber	None (N/A) (None (N/A))		
Interface	MTD-serial-SEC		

US820\_N8\_R 0 ohm I2C\_O\_LCD\_SDA 0 ohm I2C\_O\_SDA D

- I<sup>2</sup>C  
The I<sup>2</sup>C interface complies with I<sup>2</sup>C Bus Specification, Version 2.1.  
The device address is 0x2C.  
I<sup>2</sup>C clock rate: 400KHz

**KBC**  
**MFC 1515**



The slave **address** (SAD) associated to the LNG2DM is 010100xb. The **SDO/SA0** pad can be used to modify the least significant bit of the device address. If the SA0 pad is connected to a voltage supply, LSB is '1' (address 0101001b) or, if the SA0 pad is connected to ground, the LSB value is '0' (address 0101000b). This solution permits two different accelerometers to be connected and addressed to the same I<sup>2</sup>C lines.

253 SCL  
254 DIMMA

SMBus Address: 000

SCL	DIMMB
254	
SDA	DDR4

### 6.3 Address Setting

SMBus Address: 1001100xb (x is R/W bit)

---

System Management Bus (SMBus) Specification Version 3.0

## Appendix C. SMBus Device Address Assignments

Table 17. Reserved and pre-assigned SMBus addresses

Site Address	RTW Address	Description	Specification
0000 0000	0000 0000	General Call Address	PC-Bus Specification And User Manual (P.61)
0000 0000	0000 0000	START byte	PC-Bus Specification And User Manual (P.61)
0000 0001	0000 0001	CAN address	PC-Bus Specification And User Manual (P.61)
0000 0010	0000 0010	Address reserved for off-board bus terminal	PC-Bus Specification And User Manual (P.61)
0000 0011	0000 0011	Address reserved for future use	PC-Bus Specification And User Manual (P.61)
0000 1AA X	0000 1AA X	HMI Module Master Code	PC-Bus Specification And User Manual (P.61)
0001 0000	0001 0000	MIbus net	PC-Bus Specification And User Manual (P.61)
0001 0001	0001 0001	Smart Battery Charger	Smart Battery Management System V.1 1.0 December 1998
0001 010 0	0001 010 0	Smart Battery Potentiometer	Smart Battery Specification V.1 1.0 December 1998
0001 010 1	0001 010 1	Smart Battery System Manager	Smart Battery Specification V.1 1.0 December 1998
0001 011 0	0001 011 0	Smart Battery System Manager	Smart Battery Specification V.1 1.0 December 1998
0001 011 1	0001 011 1	Smart Net Response Address	System Management V.1 1.0 December 1998
0100 0000	0100 0000	Philbus - ZONE RECORD	Philbus Power System Management General Specification, Part 1 September 1998
0100 0001	0100 0001	Philbus - ZONE RECORD	Philbus Power System Management General Specification, Part 1 September 1998

CONN	7-bit Address: 0x0 0001011x x is R/W
------	---

```
SMBus Address:0b00010011(resd)
                0b00010010 (write)
```

The ISL95522 receives control inputs from the SMBus interface after Power-On Reset (POR). The serial interface complies with the System Management Bus Specification, which can be downloaded from [www.smbus.org](http://www.smbus.org). The ISL95522 uses the SMBus Read Word and Write Word protocols shown in [Figure 33 on page 32](#) to communicate with the host system and a smart battery. The ISL95522 is an SMBus slave device and does not initiate communication on the bus. It responds to the 7-bit address 0b0001001 :

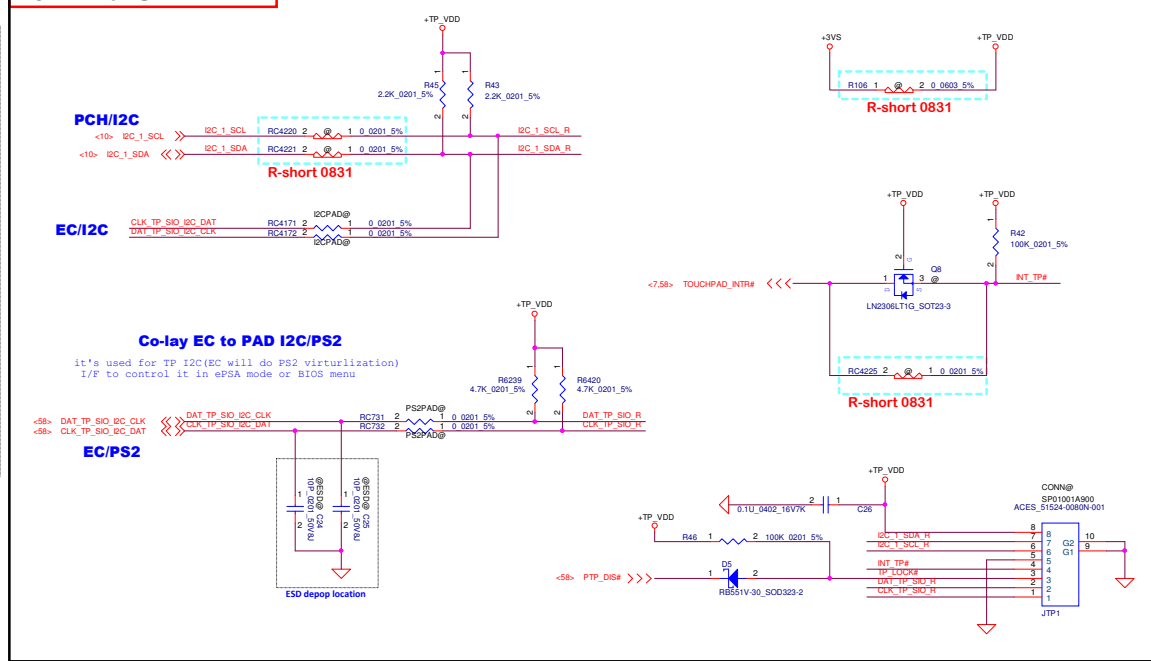
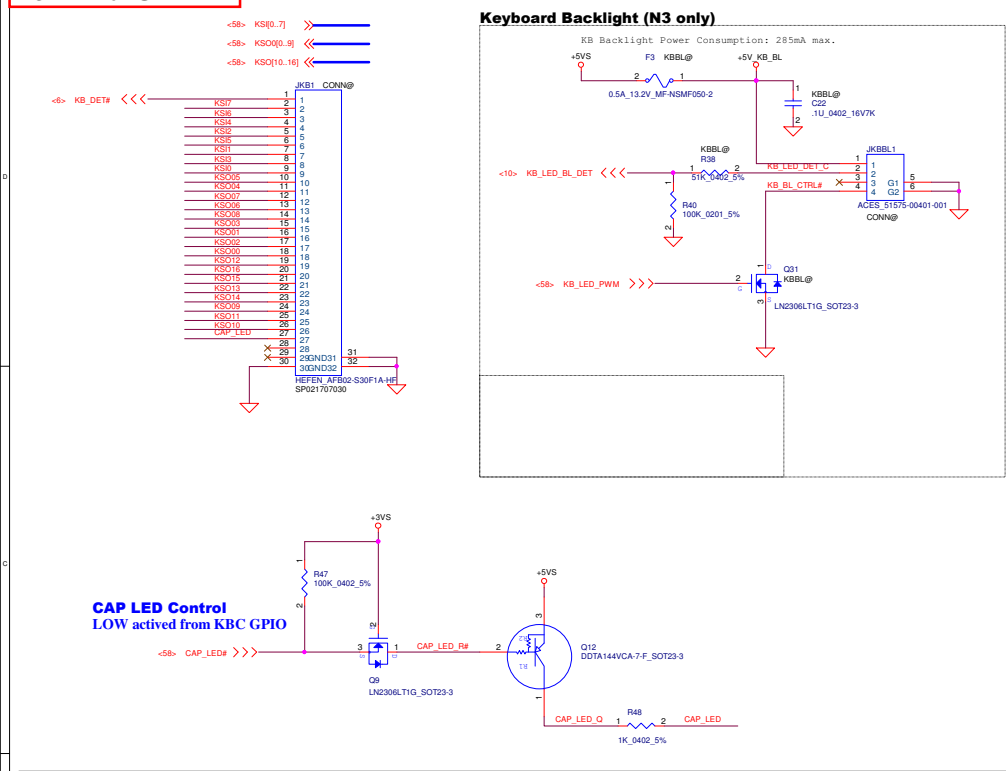
Read address = 0b00010011(0X13H)  
Write address = 0b00010010(0X12H)

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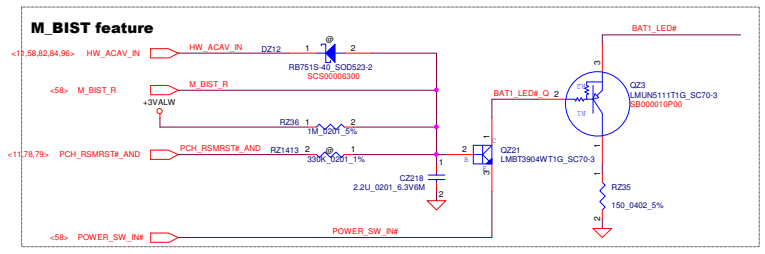
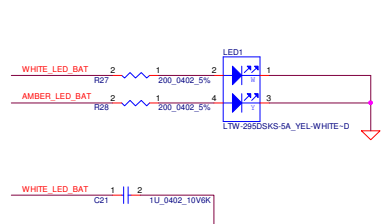
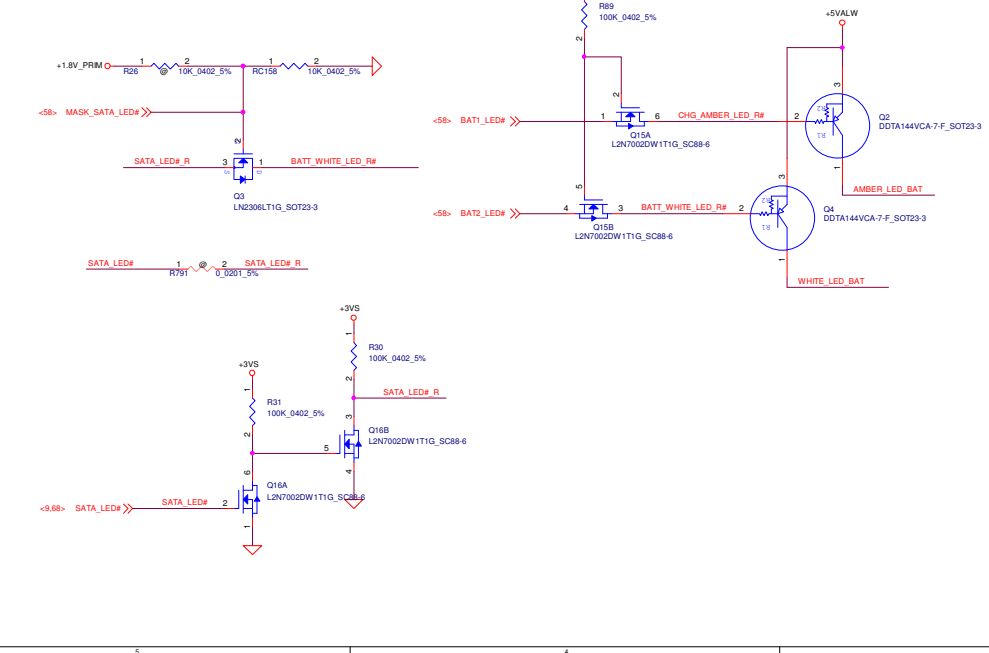
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**Main Func = Battery LED**

Low activated from KBC GPIO



Main Function:

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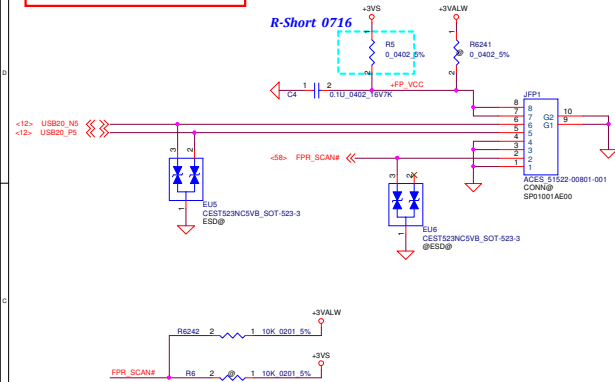
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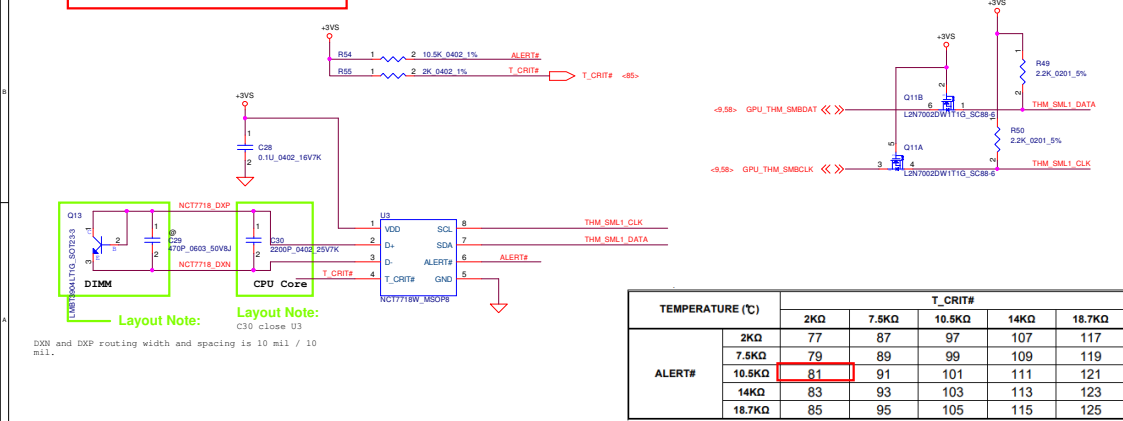
**Main Func = FPR**



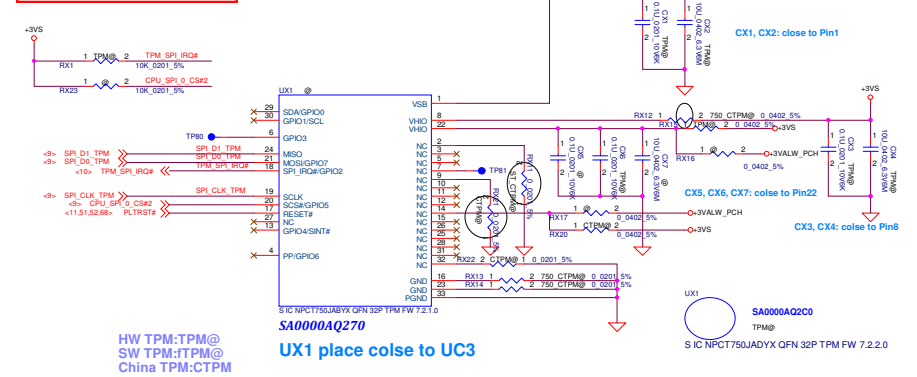
**Main Func = OTP**



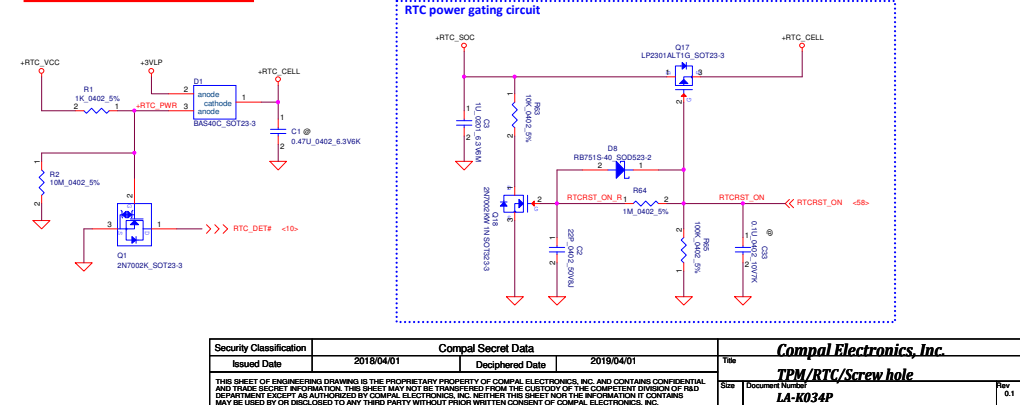
**Main Func = Thermal**



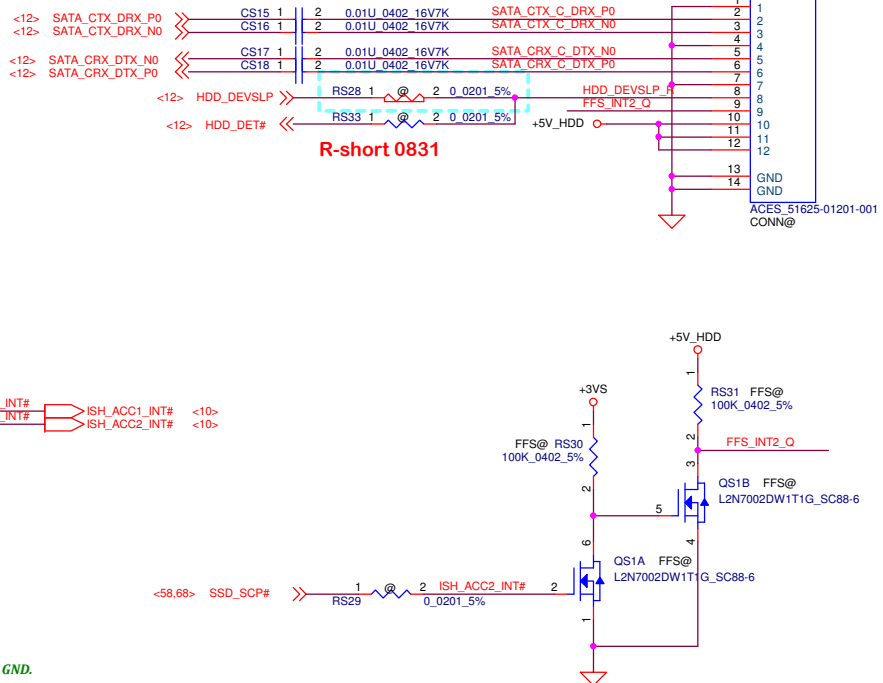
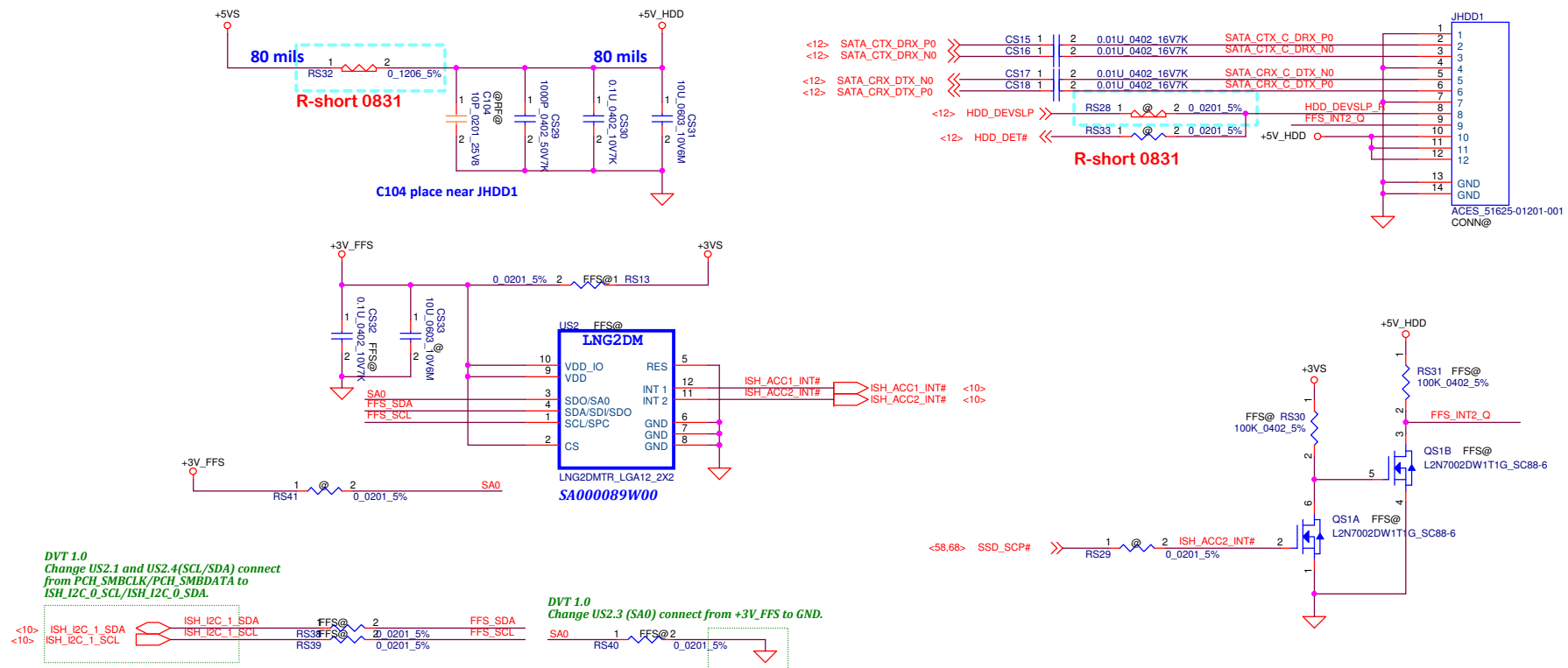
Main Func = TPM



Main Func = RTC



# Main Func = HDD&FFS



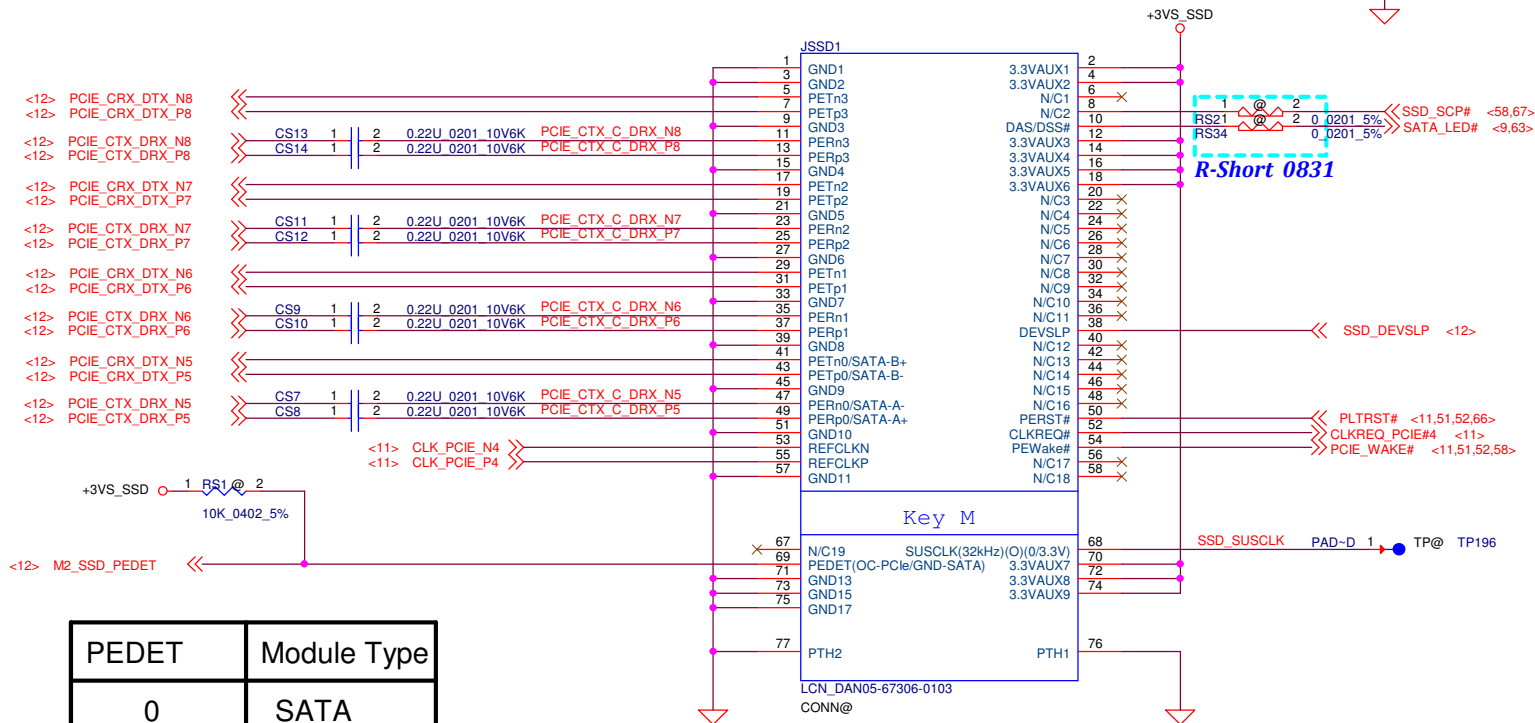
CONN		FFC
GND	S1	1
A+	S2	2
A-	S3	3
GND	S4	4
B-	S5	5
B+	S6	6
GND	S7	7
DEVSLP	P3	8
5V	P7	10
5V	P8	11
5V	P9	12
GND	P10	
Device Activity	P11	9

# Main Func = ODD

Cancel ODD

Main Func = SSD M Key CONN

NGFF Key M



PEDET	Module Type
0	SATA
1	PCIE

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Main Func = eMMC

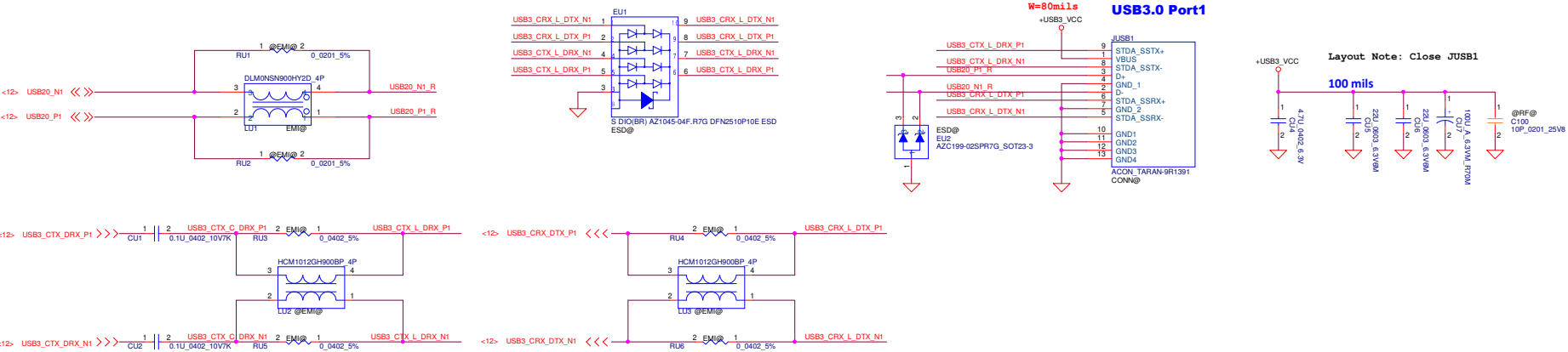
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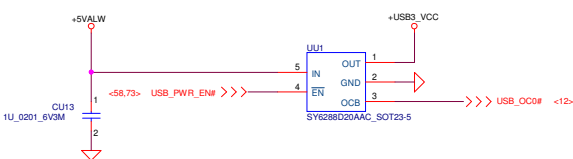
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					LA-K034P	0.1
				Date:	Monday, March 08, 2021	Sheet 70 of 101

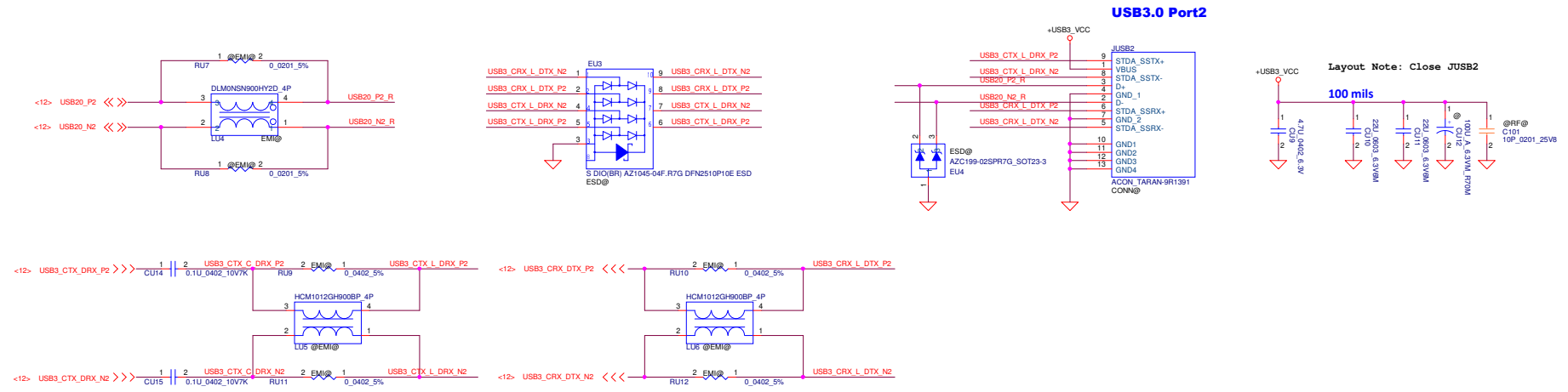
Main Func = USB3.0 Port1



Maximum Output Current 2A



Main Func = USB3.0 Port2

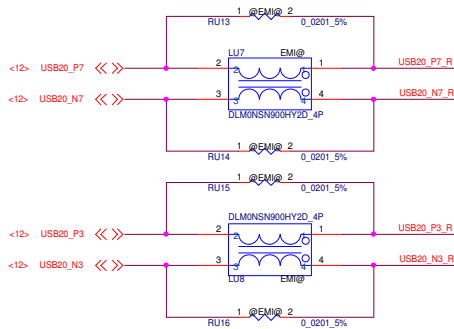
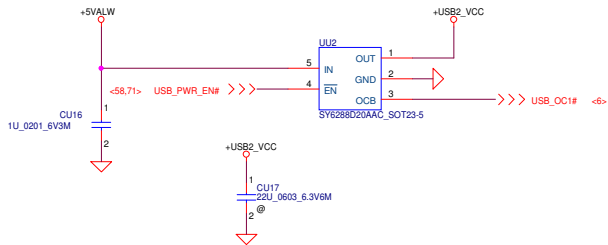


Main Function:

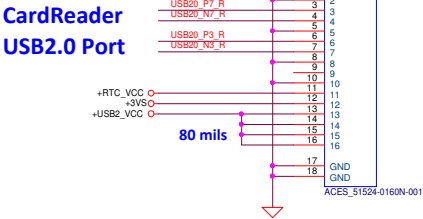
Reserve

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Main Func = USB2.0 Port3 + Card Reader on IO/B



### USB2.0/Card Reader connector



Main Function:

Reserve

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Main Function:

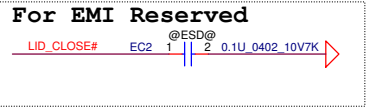
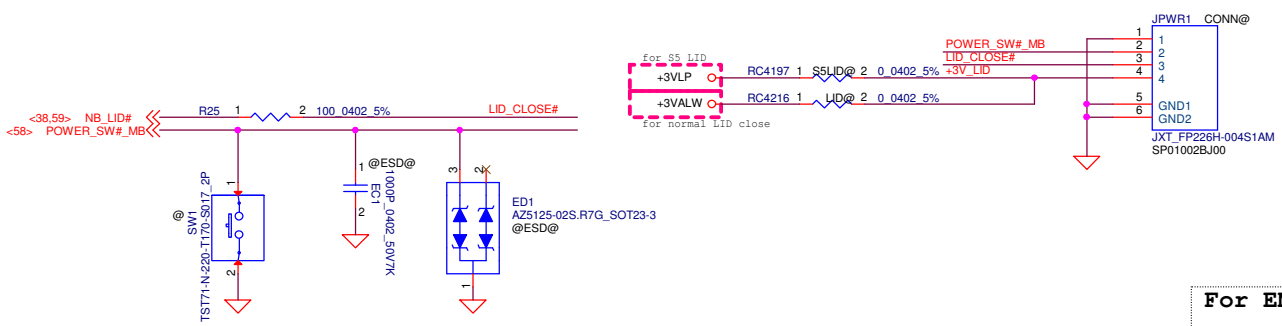
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					LA-K034P	0.1
				Date:	Monday, March 08, 2021	Sheet 76 of 101

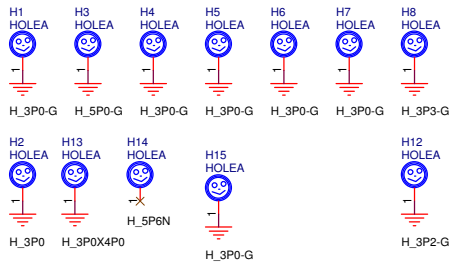


Main Func = Power BTN

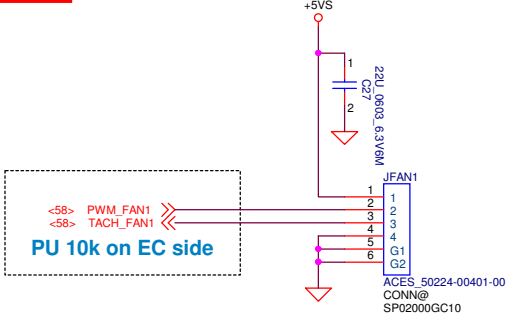
Low actived from KBC GPIO



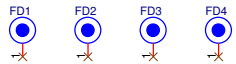
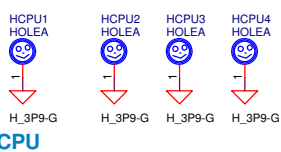
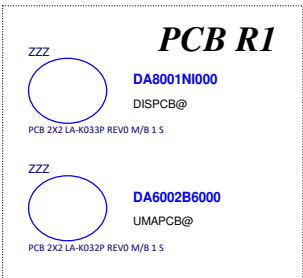
Screw hole/FD



FAN



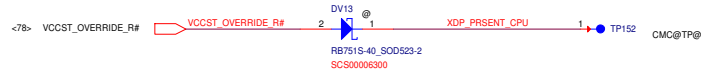
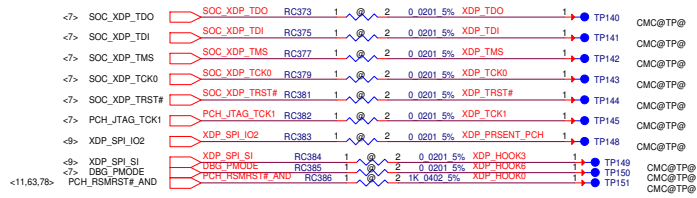
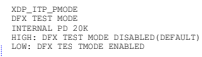
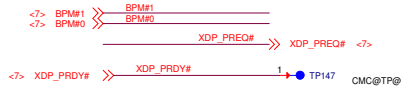
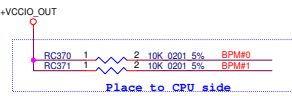
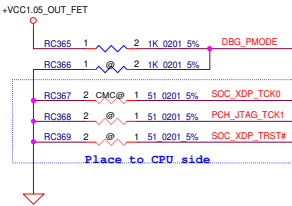
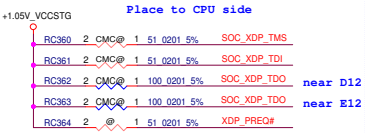
PCB PN



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								Size	Document Number	Rev
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								Date: Monday, March 08, 2021		Sheet 77 of 101



## Main Func = Debug connector



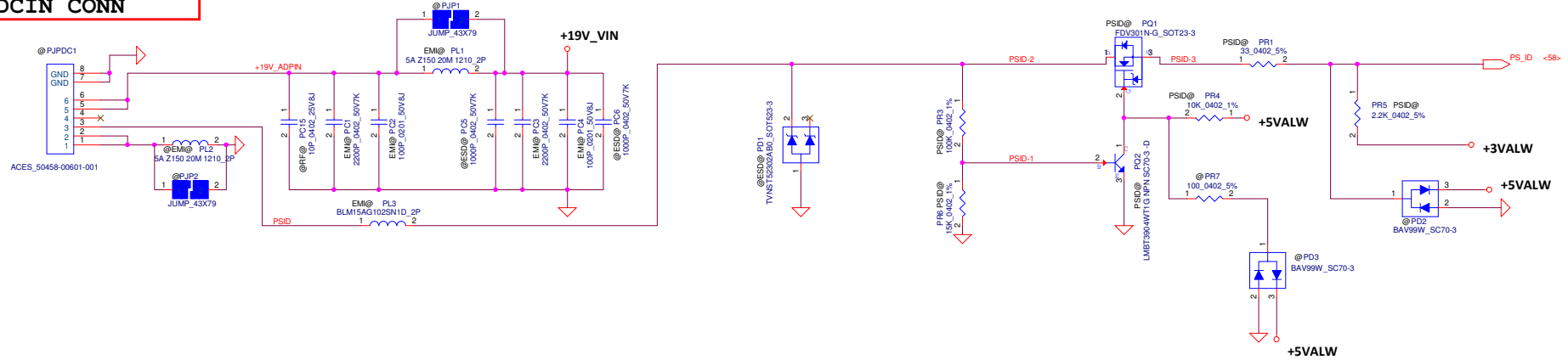
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5	4	3	2	1																											
D				D																											
C				C																											
B				B																											
A				A																											
<table><tr><td>Security Classification</td><td colspan="3">Compal Secret Data</td><td>Compal Electronics, Inc.</td></tr><tr><td>Issued Date</td><td>2018/04/01</td><td>Deciphered Date</td><td>2019/04/01</td><td>Title</td></tr><tr><td colspan="3" rowspan="2">THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&amp;D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.</td><td>Size</td><td>Document Number</td></tr><tr><td>B</td><td>LA-K034P</td></tr><tr><td colspan="3"></td><td>Date:</td><td>Monday, March 08, 2021</td></tr><tr><td colspan="3"></td><td>Sheet</td><td>80 of 101</td></tr></table>					Security Classification	Compal Secret Data			Compal Electronics, Inc.	Issued Date	2018/04/01	Deciphered Date	2019/04/01	Title	THIS SHEET OF ENGINEERING DRAWING IS THE PROPRIETARY PROPERTY OF COMPAL ELECTRONICS, INC. AND CONTAINS CONFIDENTIAL AND TRADE SECRET INFORMATION. THIS SHEET MAY NOT BE TRANSFERRED FROM THE CUSTODY OF THE COMPETENT DIVISION OF R&D DEPARTMENT EXCEPT AS AUTHORIZED BY COMPAL ELECTRONICS, INC. NEITHER THIS SHEET NOR THE INFORMATION IT CONTAINS MAY BE USED BY OR DISCLOSED TO ANY THIRD PARTY WITHOUT PRIOR WRITTEN CONSENT OF COMPAL ELECTRONICS, INC.			Size	Document Number	B	LA-K034P				Date:	Monday, March 08, 2021				Sheet	80 of 101
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				Date	Monday, March 08, 2021	Sheet 81 of 100
				Reserve for PWR		
				0.1		

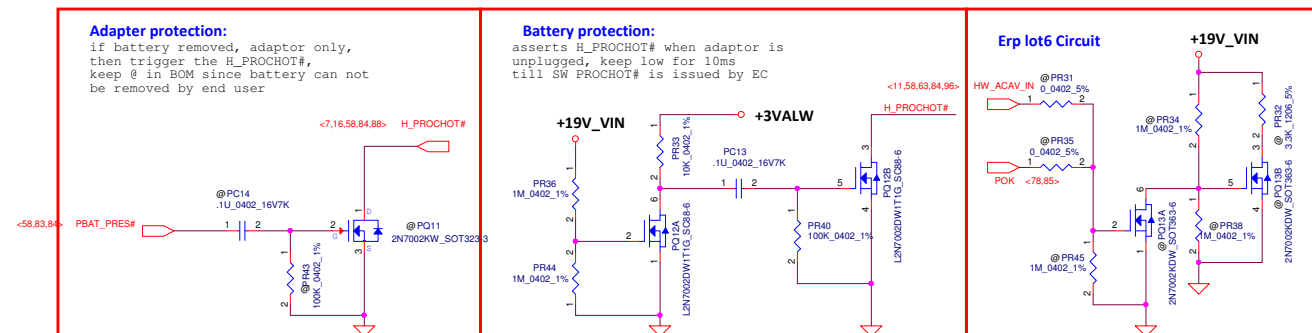
## Main Func = DCIN CONN



**Battery Bot Side**

PIN1 GND  
PIN2 GND  
PIN3 GND  
PIN4 SYS\_PRES  
PIN5 BATT\_PRS  
PIN6 DAT\_SMB  
PIN7 CLK\_SMB  
PIN8 Batt+  
PIN9 Batt+  
PIN10 Batt+  
SP021412220

ACES\_50458-01001-P01\_10P-T



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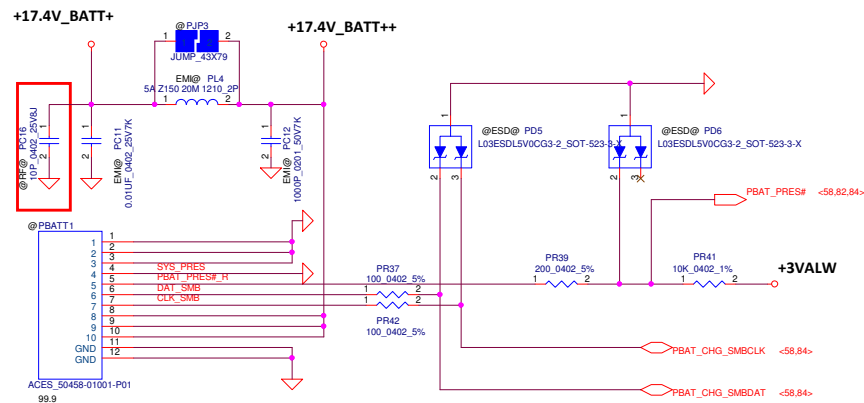
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Issued Date	2018/04/01	Deciphered Date	2019/04/01	Title	<b>PWR DCIN CONN</b>	
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Main Func = BATT CONN

### Battery Bot Side

**PIN1 GND**  
**PIN2 GND**  
**PIN3 GND**  
**PIN4 SYS\_PRES**  
**PIN5 BATT\_PRS**  
**PIN6 DAT\_SMB**  
**PIN7 CLK\_SMB**  
**PIN8 Batt+**  
**PIN9 Batt+**  
**PIN10 Batt+**  
**SP021412220**

**ACES\_50458-01001-P01\_10P-T**



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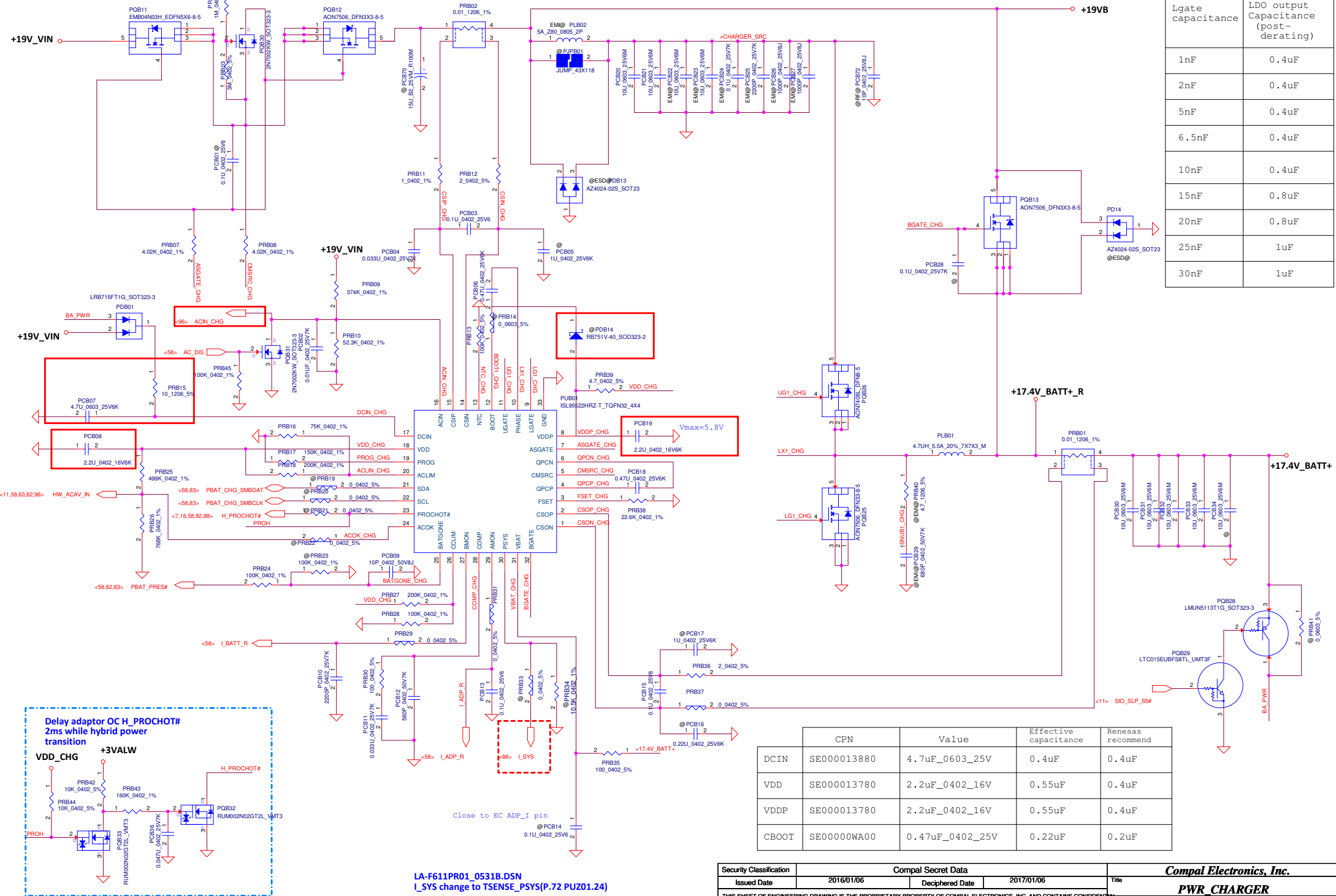
**PWR\_BATT\_CONN**[illegible]

Rev

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# Main Func = CHARGER

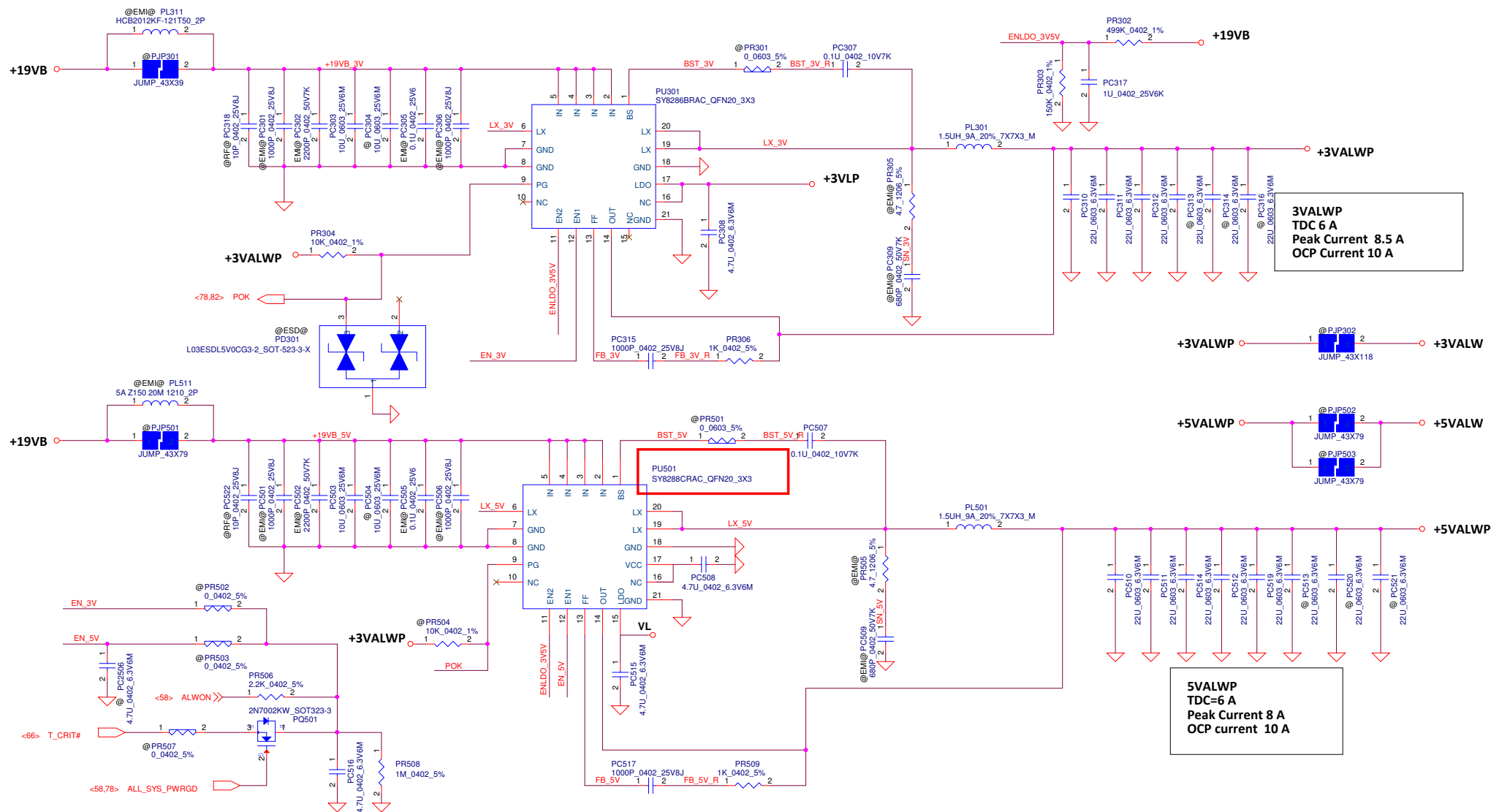


Lgate capacitance	Effective LDO output Capacitance (post-derating)
1nF	0.4uF
2nF	0.4uF
5nF	0.4uF
6.5nF	0.4uF
10nF	0.4uF
15nF	0.8uF
20nF	0.8uF
25nF	1uF
30nF	1uF

CPN	Value	Effective capacitance	Renesas recommend
DCIN	SE000013880	4.7uF_0603_25V	0.4uF
VDD	SE000013780	2.2uF_0402_16V	0.4uF
VDDP	SE000013780	2.2uF_0402_16V	0.4uF
CBOOT	SE00000WA00	0.47uF_0402_25V	0.2uF

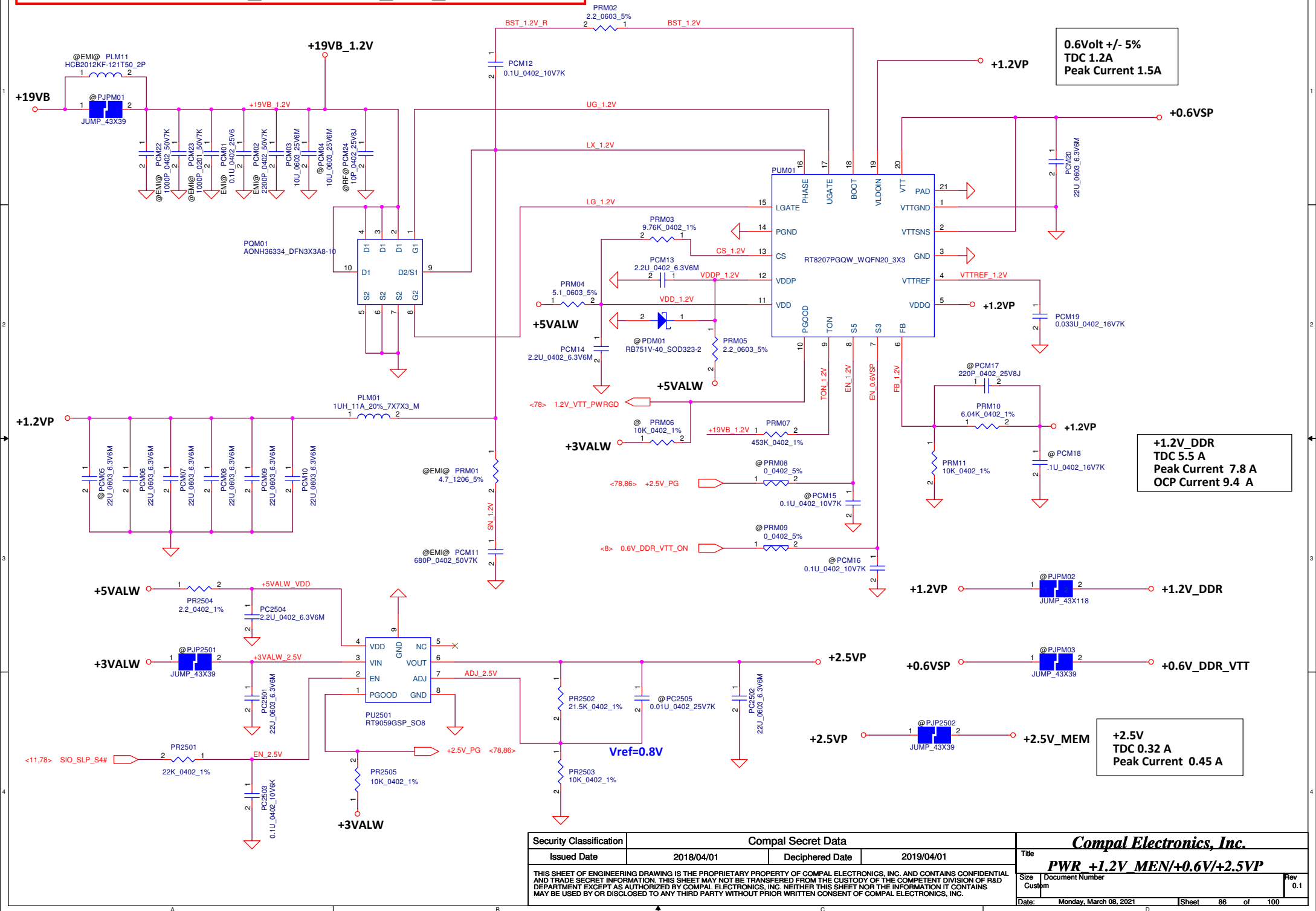


# Main Func = 3.3VALWP/5VALWP



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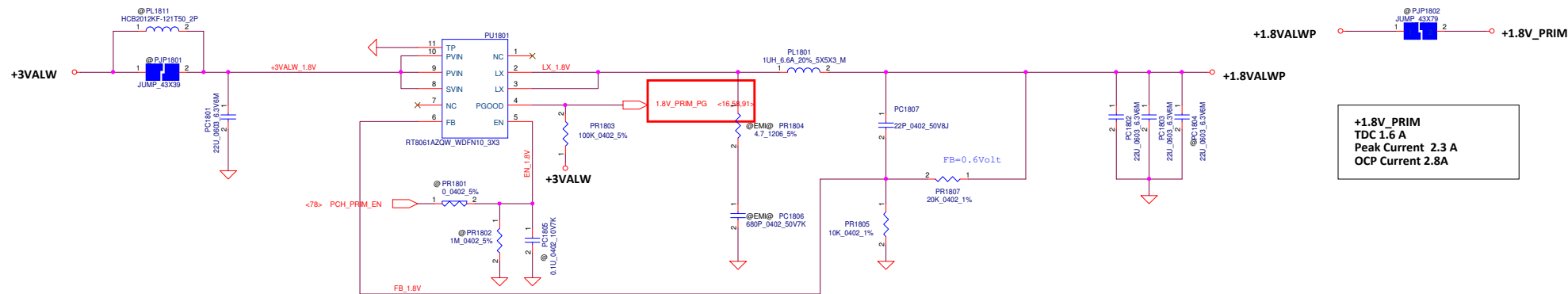
**Main Func = +1.2V\_DDR/+0.6V\_DDR\_VTT/ +2.5VP**



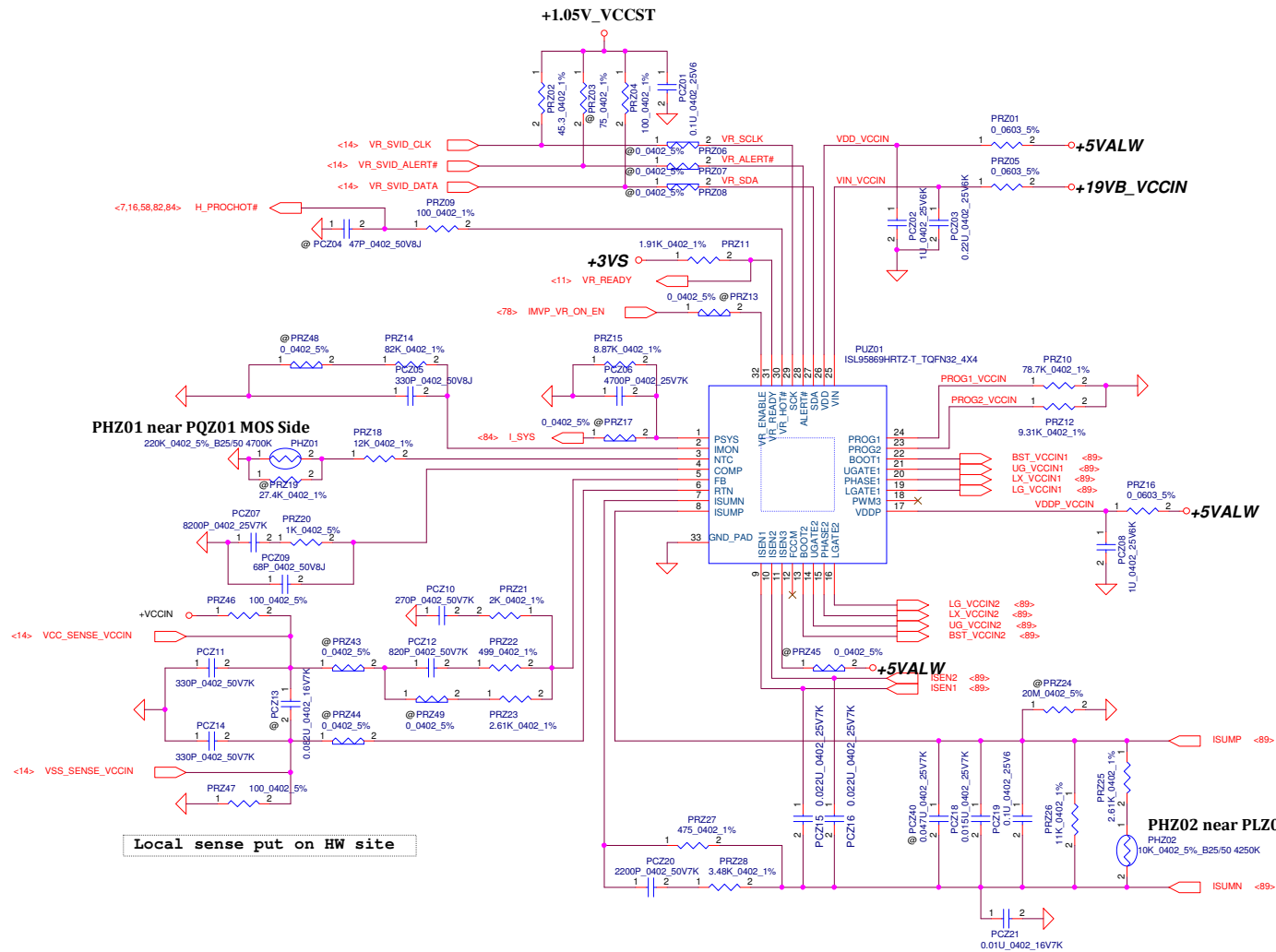
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Title			
<b>PWR +1.2V MEN/+0.6V/+2.5VP</b>			
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**Main Func = +1.8VALWP / +1.05VALWP**



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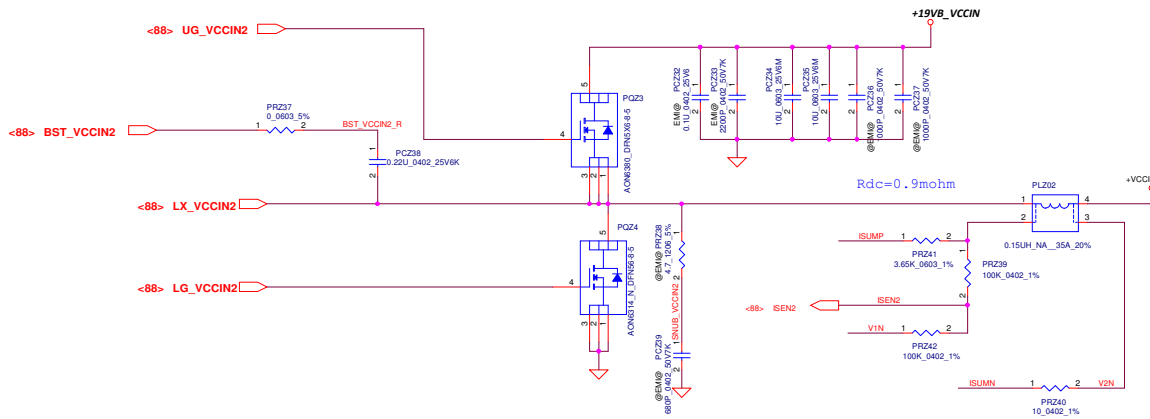
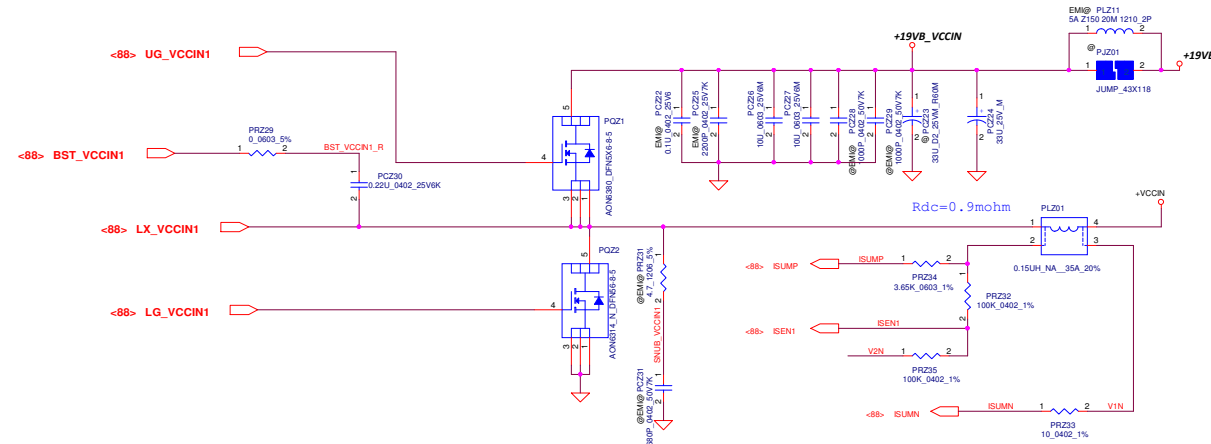
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Frequency 750KHz

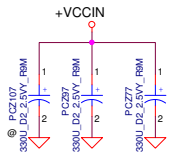
Baseline  
UP3\_4+2 15W (U42)  
ICCMAX=47A  
TDC=30A

Baseline  
UP3\_4+2 28W (U42)  
ICCMAX=55A  
TDC=36A



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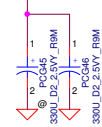
Main Func = VCCIN/ VCCIN\_AUX



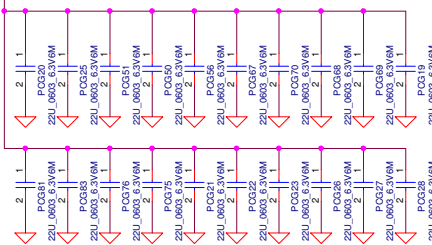
Primary side :  
330U\_R9 \*2  
22U\_0603 \*14

+VCCIN\_AUX

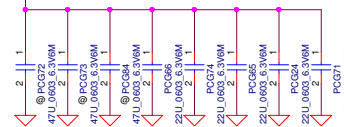
330U\_R9 \*1  
22U\_0603 \*25



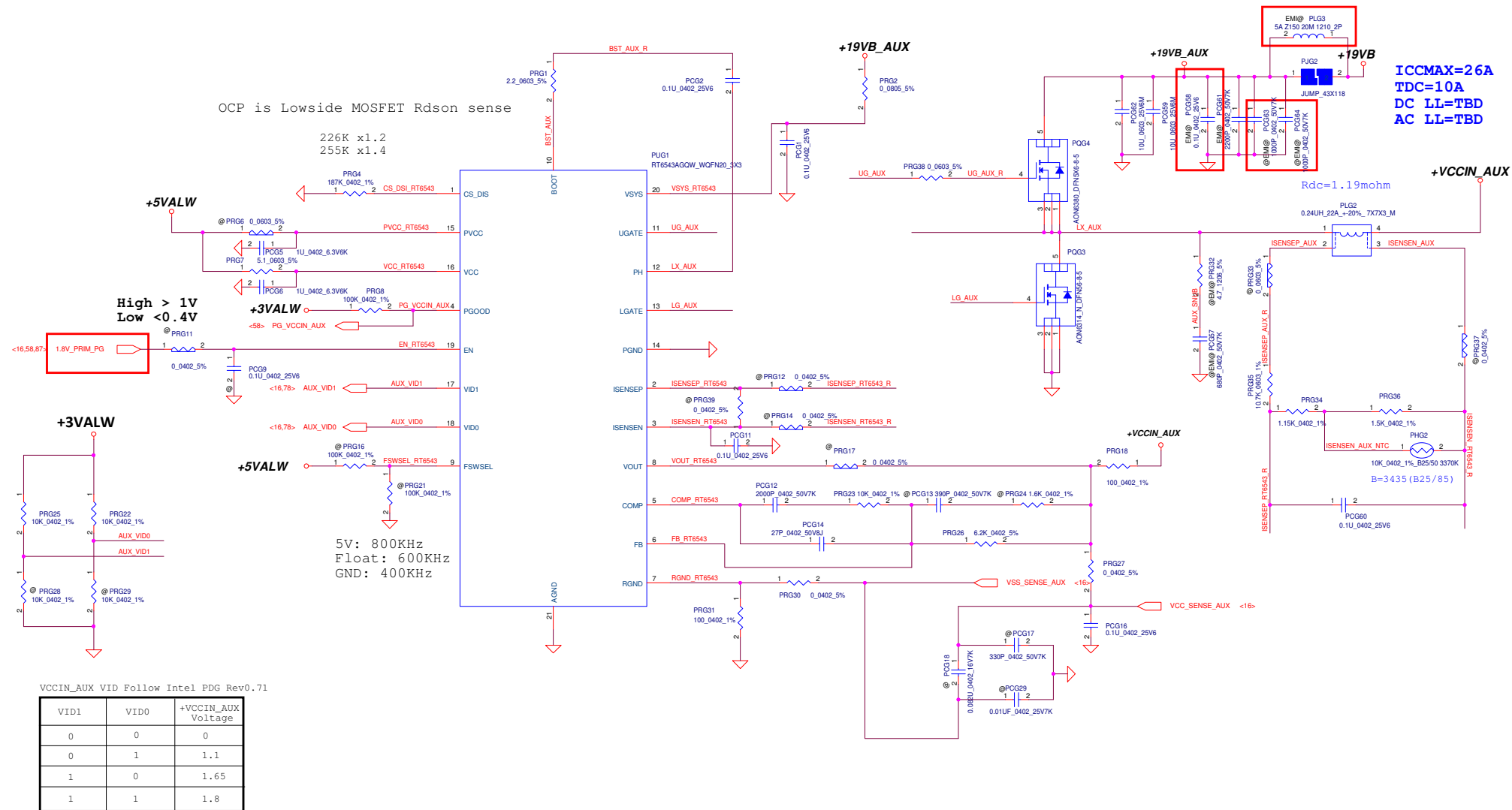
+VCCIN\_AUX



+VCCIN\_AUX



**Main Func = VCCIN\_AUX**



VID1	VID0	+VCCIN_AUX Voltage
0	0	0
0	1	1.1
1	0	1.65
1	1	1.8

# Reserve

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						0.1
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Version Change List ( P. I. R. List )

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	P83	BATT CONN	20190423	COMPAL	RF request for RF test	Reserve PC16	0.2 (X01)
2	P84	PWR CHARGER	20190423	COMPAL	"Based on Loki G issue, change to follow Renesas recommendation "	1. PCB07 change to 0603 2. Remove PCB71 3. PRB15 change to 1206	0.2 (X01)
3	P96	NO SMOKE	20190423	COMPAL	customer request	Add page 96: reserve NO SMOKE schematic	0.2 (X01)
4	P88	PWR VCCIN	20190507	COMPAL	Change RC value for Intel EA test	"Change RC value for Intel test:  PCZ77=330UF PCZ79/80/81/82/84/85/86/87/90/96/98/99/100/102=22uF  VCCAUX Output caps 1+9 PCG46=330UF PCG19/24/28/50/51/65/71/75/76=22uF  PRZ14/25=2.21Kohm PRZ13/24=2.05kohm PRZ17/26=3.01Kohm PRZ48=37.4Kohm PRZ66=200ohm PRZ49=12.1Kohm PRZ53=14.7kohm PCZ10=82pF PCZ11=220pF "	0.2 (X01)



DVT1 EE change list

Design Change								
Item	Date	Page	Part reference	Change description	Reason	Schematic	Bom	Layout
Based on 05/15								
1	2018/5/17	8		Add RC207, CPU_SPL_0_CS#1	For 2nd ROM	Y	N	Y
2	2018/5/17	66		Del JP7, short +5VS and +5VS_ODD	Optimal B+ routing	Y	N	Y
3	2018/5/17	14		CC52,CC48,CC51,CS change to 0402	meet purchase requirement	Y	Y	Y
4	2018/5/17	29		CV73-CV78, CV100-CV109 change to 0402	meet purchase requirement	Y	Y	Y
5	2018/5/17	71		del CU3,CU8 CU4,CU9 IU change to 4.7U	meet purchase requirement	Y	Y	Y
6	2018/5/20			Del CS6,CU3,CU8; CU13,CU16,C8,C35,C39 change to 0201,CT1 change to 0603	MLCC downsize	Y	Y	Y
7	2018/5/25			Del C34,R68,R69,R70,R71; U2 change Footprint	For 17" Touch	Y	N	Y
8	2018/6/4	38		Connect UC1,CC30 to R72, Add RC208,RC209	For 17" Touch	Y	N	Y
9	2018/6/4			C27,CT14,CU10,CU11,CU5,CU6,CU17 change to 0603	MLCC downsize	Y	Y	Y
10	2018/6/4	31		CV161,CV162,CV163,CV164,CV165,CV166,CV167,CV168,CV169,CV170,CV182,CV183,CV184,CV185,CV186,CV187,CV188,CV189,CV190,CV191,CL16 change to 0201	MLCC downsize	Y	Y	Y
11	2018/6/13	56		CA16 change to 0402	MLCC downsize	Y	Y	Y
12	2018/7/4	65		add Rx10~14	co-lay ST TPM	Y	N	Y
13	2018/7/4			add CC75(pop),CZ41,CC76,CC77,CC78,CC79	For ESD requirement	Y	Y	Y
14	2018/7/6	65		add Rx15~RX19	co-lay China TPM	Y	N	Y

DVT2 EE change list

Design Change								
Item	Date	Page	Part reference	Change description	Reason	Schematic	Bom	Layout
Based on 07/16								
1	2018/8/14	66	RX20,RX21,RX22	reserve 0 ohm 0402	reserve for china TPM	Y	N	Y
2	2018/8/15	38	R96	reserve 0 ohm 0201	disconnct B+	Y	N	Y
3			EU1,EU3,EU8,EU9	SC300002C00=>SC300001Y00	ESD require	Y	Y	N
4		71	RE1	SD034178280=>SD034270280 17.8K change to 27K	EC board ID	Y	Y	N
5			CC54,CC57		fixed 1.05 OVPUBITS382716)	Y	Y	N
6			UZ2	SA00007XR00=>SA00008R600(Vccio load switch)	fixed 1.05 OVPUBITS382716)	Y	Y	N
7				Remove Typec configuration	Dell PCR	N	Y	N
8			CC64,CC52,CC59,CC17,CC15,CC18,CC19	0402 1u =>0201 1u	MLCC downsize	Y	Y	Y
9			R52	7.15K =>6.49K	Fixed OTP issue(BITS383003)	Y	Y	N